K.S.Rangasamy College of Technology

(Autonomous)

Curriculum & Syllabi

of

M.E. VLSI Design

(For the batch admitted in 2022 – 2023)

R 2022

Accredited by NAAC with 'A++' Grade, Approved by AICTE,
Affiliated to Anna University, Chennai.

KSR Kalvi Nagar, Tiruchengode – 637 215.
Namakkal District, Tamil Nadu, India.

Vision

To become recognized as a leader in Electronics and Communication Engineering education and research

Mission

- To craft professionals and technology leaders adherent to the professional ethical code in the areas of Electronics and communication Engineering
- To address the needs of the society while advancing boundaries of disciplinary and multidisciplinary research and cultivate universal moral values

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: To develop a progressive career in research and industry with the ability to analyse, design and fabricate Integrated Circuits.

PEO2: To gain a firm grasp on growing areas of VLSI with acquired knowledge on concepts and use of appropriate tools

PEO3: To exhibit ethical practices and social behavior with an attitude of lifelong learning and strong communication skills

PROGRAMME OUTCOMES (POs)
Engineering Graduates will be able to:

PO1: An ability to independently carry out research /investigation and development work to solve practical problems
PO2: An ability to write and present a substantial technical report/document
PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4: An ability to identify appropriate EDA tool for design and analysis of Integrated Circuits
PO5: An ability to communicate effectively and solve societal problems with ethical principles
PO6: An ability to apply the knowledge of VLSI concepts in the design and development of Integrated Circuits

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MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES (PEOs) WITH PROGRAMMEOUTCOMES (POs)

The M.E. VLSI Design Programme outcomes leading to the achievement of the objectives are summarized in the following Table.

Programme Educational Objectives	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
PEO 1	3	3	3	3	3	2
PEO 2	3	3	3	3	3	3
PEO 3	2	2	2	2	2	3

Contributions: 1- low, 2- medium, 3- high

MAPPING: VLSI DESIGN(PG)

YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6
I	I	60 PVL 101	Graph Theory and Optimization Techniques	3	3	2.6	2.6	2.6	3
		60 PED 001	Research Methodology and IPR	3	3	2	2	2	2
		60 PVL 103	Analog IC Design	3	3	3	2	2	3
		60 PVL 104	Digital CMOS VLSI Design	3	3	2.8	2.8	3	3
		60 PVL 105	Advanced Digital System Design	3	3	3	3	3	3
		60 PVL 106	Advanced Embedded Computing	3	3	3	3	3	2
		60 AT 001	English for Research Paper Writing						
		60 PVL1P1	VLSI Laboratory I	3		3	3	3	3
		60 PVL1P2	Analog IC Design Laboratory	3	3	3	3	2	3
	II	60 PVL 201	Design for Verification using UVM	3		3	3		3
		60 PVL 202	Low Power VLSI Design	3		3	2.5		3
		60 PVL 203	RF Circuit Design	3	3	3	3	2	3
		60 PVL 204	VLSI Testing	3		3	2.7		3
		60 PVL E1*	Professional Elective I						
		60 PVL E2*	Professional Elective II						
		60 AT 002	Disaster Management						
		60 PVL 2P1	VLSI Laboratory II	3		3	3	3	3
		60 PVL 2P2	Term Paper and Seminar	3	2.75	3	2.4	2.75	3
II	III	60 PVL 301	VLSI Signal Processing	3	3	3	2.4	2.6	3
		60 PVL E3*	Professional Elective III						
		60 PVL E4*	Professional Elective IV						
		60 PVL 3P1	Project Work I	3	3	3	3	3	3
	IV	60 PVL 4P1	Project Work II	3	3	3	3	3	3

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PROFESSIONAL CORE (PC)

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL 101	Graph Theory and Optimization Techniques	PC	5	3	2	0	4	Nil
2.	60 PED 001	Research Methodology and IPR	RM	3	3	0	0	3	Nil
3.	60 PVL 103	Analog IC Design	PC	3	3	0	0	3	Semiconductor Devices and Circuits and Linear IC Applications
4.	60 PVL 104	Digital CMOS VLSI Design	PC	3	3	0	0	3	Digital logic design, VLSI Design
5.	60 PVL 105	Advanced Digital System Design	PC	5	3	2	0	4	Digital Logic Design
6.	60 PVL 106	Advanced Embedded Computing	PC	3	3	0	0	3	Embedded Systems
7.	60 PVL1P1	VLSI Laboratory I	PC	4	0	0	4	2	Analog and Digital CMOS VLSI design
8.	60 PVL1P2	Analog IC Design Laboratory	PC	4	0	0	4	2	Semiconductor Devices and Circuits and Linear IC Applications
9.	60 PVL 201	Design for Verification using UVM	PC	3	3	0	0	3	System Verilog
10.	60 PVL 202	Low Power VLSI Design	PC	3	3	0	0	3	Analog and Digital CMOS VLSI design
11.	60 PVL 203	RF Circuit Design	PC	3	3	0	0	3	RF Passive and Active Devices, Transmission Lines.
12.	60 PVL 204	VLSI Testing	PC	3	3	0	0	3	Analog and Digital CMOS VLSI design
13.	60 PVL 2P1	VLSI Laboratory II	PC	4	0	0	4	2	Basic Verilog HDL
14.	60 PVL 2P2	Term Paper and Seminar	CG	2	0	0	2	0	Nil
15.	60 PVL 301	VLSI Signal Processing	PC	3	3	0	0	3	Nil

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PROFESSIONAL ELECTIVE (PE)

SEMESTER II, PROFESSIONAL ELECTIVE I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL E11	Nano Electronics	PE	3	3	0	0	3	Nil
2.	60 PVL E12	Linear Algebra	PE	3	3	0	0	3	Basic Linear Algebra
3.	60 PVL E13	Digital image Processing	PE	3	3	0	0	3	Nil
4.	60 PVL E14	IP based VLSI Design	PE	3	3	0	0	3	Digital CMOS VLSI Design
5.	60 PVL E15	Genetic algorithm for VLSI Design	PE	3	3	0	0	3	Digital CMOS VLSI Design
6.	60 PVL E16	Bio Signal Processing	PE	3	3	0	0	3	Digital Signal Processing

SEMESTER II, PROFESSIONAL ELECTIVE II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL E21	VLSI for wireless communication	PE	3	3	0	0	3	Fundamentals of VLSI and Wireless Communication
2.	60 PVL E22	System On Chip	PE	3	3	0	0	3	Nil
3.	60 PVL E23	Machine Learning Techniques	PE	3	3	0	0	3	Nil
4.	60 PVL E24	FPGA based implementation of signal processing systems	PE	3	3	0	0	3	Digital Logic Design and Digital Signal processing
5.	60 PVL E25	Network on Chip	PE	3	3	0	0	3	Interconnection Networks
6.	60 PVL E26	Wireless Sensor Networks	PE	3	3	0	0	3	Nil

SEMESTER III, PROFESSIONAL ELECTIVE III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL E31	DSP Structures for VLSI	PE	3	3	0	0	3	Signal processing
2.	60 PVL E32	Applied medical image processing	PE	3	3	0	0	3	Image processing
3.	60 PVL E33	Data Science and Engineering	PE	3	3	0	0	3	Linear algebra, Statistics
4.	60 PVL E34	ASIC Design	PE	3	3	0	0	3	Digital logic design
5.	60 PVL E35	Mixed Signal VLSI design	PE	3	3	0	0	3	Analog and digital CMOS design

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SEMESTER III, PROFESSIONAL ELECTIVE IV

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL E41	System Verilog	PE	5	3	0	2	4	Verilog
2.	60 PVL E42	HDL for IC design	PE	5	3	0	2	4	Verilog
3.	60 PVL E43	Deep learning	PE	5	3	0	2	4	Linear algebra
4.	60 PVL E44	Adaptive Signal Processing	PE	5	3	0	2	4	Signal processing
5.	60 PVL E45	MEMS system design	PE	5	3	0	2	4	Electronic Circuits

RESEARCH METHODOLOGY (RM)

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PED 001	Research Methodology and IPR	RM	3	3	0	0	3	Nil

AUDIT COURSES (I/II) (AC)

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 AT 001	English for Research Paper Writing	AC	2	2	0	0	0	Nil
2	60 AT 002	Disaster Management	AC	2	2	0	0	0	Nil
3.	60 AT 003	Constitution of India	AC	2	2	0	0	0	Nil

CAREER GUIDANCE COURSES (CG)

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 PVL 2P2	Term Paper and Seminar	CG	2	0	0	2	0	Nil
2.	60 PVL 3P1	Project Work I	CG	12	0	0	12	6	Nil
4.	60 PVL 4P1	Project Work II	CG	24	0	0	24	12	Nil

SUMMARY

S.No.	Category	Credits per semester				Total Credits	Percentage%
		I	II	III	IV		
1.	PC	21	14	3	-	38	52.7
2.	PE	-	6	7	-	13	18.0
3.	RM	3	-	-	-	03	0.04
4.	CG	-	-	6	12	18	25.0
5.	AC	AC I	AC II	-	-	-	-
Total		24	20	16	12	72	100

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SEMESTER I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 PVL 101	Graph Theory and Optimization Techniques	PC	5	3	2	0	4
2.	60 PED 001	Research Methodology and IPR	RM	3	3	0	0	3
3.	60 PVL 103	Analog IC Design	PC	3	3	0	0	3
4.	60 PVL 104	Digital CMOS VLSI Design	PC	3	3	0	0	3
5.	60 PVL 105	Advanced Digital System Design	PC	5	3	2	0	4
6.	60 PVL 106	Advanced Embedded Computing	PC	3	3	0	0	3

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7.	60 PAC 001	English for Research Paper Writing	AC	2	2	0	0	0
PRACTICALS								
8.	60 PVL 1P1	VLSI Laboratory I	PC	4	0	0	4	2
9.	60 PVL 1P2	Analog IC Design Laboratory	PC	4	0	0	4	2
			TOTAL	**32**	**20**	**4**	**8**	**24**

SEMESTER II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 PVL 201	Design for Verification using UVM	PC	3	3	0	0	3
2.	60 PVL 202	Low Power VLSI Design	PC	3	3	0	0	3
3.	60 PVL 203	RF Circuit Design	PC	3	3	0	0	3
4.	60 PVL 204	VLSI Testing	PC	3	3	0	0	3
5.	60 PVL E1*	Professional Elective I	PE	3	3	0	0	3
6.	60 PVL E2*	Professional Elective II	PE	3	3	0	0	3
7.	60 PAC 002	Disaster Management	AC	2	2	0	0	0
PRACTICALS								
8.	60 PVL 2P1	VLSI Laboratory II	PC	4	0	0	4	2
9.	60 PVL 2P2	Term Paper and Seminar	CG	2	0	0	2	0
			TOTAL	**26**	**20**	**0**	**6**	**20**

SEMESTER III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 PVL 301	VLSI Signal Processing	PC	3	3	0	0	3
2.	60 PVL E3*	Professional Elective III	PE	3	3	0	0	3
3.	60 PVL E4*	Professional Elective IV	PE	5	3	0	2	4
PRACTICALS								
4.	60 PVL 3P1	Project Work I	CG	12	0	0	12	6
			TOTAL	**23**	**9**	**0**	**14**	**16**

SEMESTER IV

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1.	60 PVL 4P1	Project Work II	CG	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTALCREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE: 72

Note: PC-Professional Core Courses, PE-Professional Elective Courses, RM- Research Methodology, CG -Career Guidance Courses, AC- Audit Courses

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M.E. / M.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted from 2022-2023 onwards)

FIRST SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 PVL 101	Graph Theory and Optimization Techniques	2	40	60	100	45	100
2.	60 PED 001	Research Methodology and IPR	2	40	60	100	45	100
3.	60 PVL 103	Analog IC Design	2	40	60	100	45	100
4.	60 PVL 104	Digital CMOS VLSI Design	2	40	60	100	45	100
5.	60 PVL 105	Advanced Digital System Design	2	40	60	100	45	100
6.	60 PVL 106	Advanced Embedded Computing	2	40	60	100	45	100
7.	60 AT 001	English for Research Paper Writing	2	100	-	100	-	100
PRACTICAL								
8.	60 PVL1P1	VLSI Laboratory I	3	60	40	100	45	100
9.	60 PVL1P2	Analog IC Design Laboratory	3	60	40	100	45	100

SECOND SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 PVL 201	Design for Verification using UVM	2	40	60	100	45	100
2.	60 PVL 202	Low Power VLSI Design	2	40	60	100	45	100
3.	60 PVL 203	RF Circuit	2	40	60	100	45	100

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		Design						
4.	60 PVL 204	VLSI Testing	2	40	60	100	45	100
5.	60 PVL E1*	Professional Elective I	2	40	60	100	45	100
6.	60 PVL E2*	Professional Elective II	2	40	60	100	45	100
7.	60 AT 002	Disaster Management	2	100	-	100	-	100
PRACTICAL								
8.	60 PVL 2P1	VLSI Laboratory II	3	60	40	100	45	100
9.	60 PVL 2P2	Term Paper and Seminar	3	100	00	100	-	100

THIRD SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 PVL 301	VLSI Signal Processing	2	40	60	100	45	100
2.	60 PVL E3*	Professional Elective III	2	40	60	100	45	100
3.	60 PVL E4*	Professional Elective IV	2	40	60	100	45	100
PRACTICAL								
4.	60 PVL 3P1	Project Work I	2	100	00	100	-	100

FOURTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
PRACTICAL								
1.	60 PVL 4P1	Project Work II	2	60	40	100	45	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for the award of terminal examination marks

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60 PVL 101	GRAPH THEORY AND OPTIMIZATION TECHNIQUES

Category	L	T	P	Credit
PC	3	2	0	4

Objective

- To know and apply the fundamental concepts in graph theory.
- To learn the model problems using graphs and to solve these problems algorithmically.
- To expose the concepts of modeling and optimization for solving real world problems.
- To study a systematic procedure for determining the optimal combination of decisions of dynamic programming.
- To learn the mathematical foundations of the genetic algorithm and ant colony optimization in the field of communication engineering.

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the basic terminology and some of the theory associated with graphs.	Remember, Understand, Apply
CO2	Formulate graph theoretic models to solve real world problems.	Remember, Understand, Apply
CO3	Explain the linear programming principles and its conversion.	Remember, Understand, Apply
CO4	Conceptualize the principle of optimality and sub-optimization, formulatio and computational procedure of dynamic programming.	Remember, Understand, Apply
CO5	Analyze the Genetic based machine learning and its applications.	Remember, Understand, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	
CO2	3	3	2	2	2	
CO3	3	3	3	3	3	
CO4	3	3	3	3	3	
CO5	3	3	3	3	3	
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)			End Sem Examination (Marks)
	1	2	Model Exam (Marks)	
Remember (Re)	14	6	12	10
Understand (Un)	14	6	12	10
Apply (Ap)	32	48	76	80
Analyze (An)	--	--		--
Evaluate (Ev)				
Creative (Cr)	--	--		--
Total	60	60	100	100

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60 PVL 101- GRAPH THEORY AND OPTIMIZATION TECHNIQUES								
M.E-VLSI Design								
Semester	Hours/Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	2	0	60	4	40	60	100

Basic Concepts In Graph Theory Undirected graph — Degree of a vertex - Degree sequence - Sub graphs - Vertex induced sub graphs - Complement of a graph - Self complementary graphs – Walk – Path – Connectivity – Eccentricity – Radius – Diameter - Vertex and edge cuts - Vertex partition - Independent set - Clique. Digraph — Orientation – Strongly connected digraphs – Weekly connected digraphs - Unilaterally connected digraphs - Directed acyclic graph. Adjacency matrix - Incidence matrix of graphs. Trees - Spanning trees - Matrix tree theorem.	[9]
Graph algorithms Search algorithms — Depth first search and breadth first search - Spanning tree algorithm — Kruskal's and Prim's shortest path algorithm — Dijkstra's and Floyd-Marshall. Matching — Perfect matching, Bipartite matching. Flow networks — Augmenting path algorithm - Min-cut and max-cut algorithms.	[9]
Linear Programming Formulation of linear programming problem - Graphical method - Simplex method - Two phase method - Big M-method - Duality - Dual simplex method.	[9]
Integer and Dynamic Programming Integer programming problem - Pure and mixed integer – Gomory's cutting plane algorithm. Dynamic programming problem - Principle of optimality - Backward and forward induction methods - Calculus method of solution - Tabular method of solution - Shortest path network problems - Applications in production.	[9]
Nontraditional Optimization Algorithms Genetic Algorithm — Working Principle — Comparison between GA and traditional method — GA operators - GA for constrained optimization. Ant colony optimization - Ant's foraging behavior and optimization - Artificial ants and minimum cost paths - Traveling salesman problem - ACO algorithm for traveling salesman problem.	[9]
Total Hours: 45 + 15(Tutorial)	**60**

TextBook(s):

1. Jonathan L Gross and Jay Yellen, 'Graph Theory and its Applications', Chapman & Hall, New York, 2005.
2. Hamdy A Taha, 'Operations Research. An Introduction', Pearson Education, New Delhi, 2014.

Reference(s):

1. West D B, 'Introduction To Graph Theory', Pearson Education, New Delhi, 2007.
2. KantiSwarup, P.K.Gupta, Man Mohan, ' Operations Research',12th Edition, Sultan Chand & Sons, New Delhi, 2004.
3. Kalyanmoy Deb, 'Optimization for Engineering Design, Algorithms and Examples', Prentice Hall, New Delhi, 2010.
4. Marco Dorigo and Thomas Stutzle, 'Ant Colony Optimization', Prentice Hall, New Delhi, 2005.

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Course Contents and Lecture Schedule

S. No	Topic	No. of Hours
1	**Basic Concepts In Graph Theory**	
1.1	Undirected graph, Degree of a vertex, Degree sequence	2
1.2	Sub graphs, Vertex induced sub graphs, Complement of a graph	1
1.3	Self complementary graphs, Walk, Path, Connectivity	1
1.4	Eccentricity, Radius, Diameter, Vertex and edge cuts, Vertex partition	1
1.5	Tutorial	2
1.6	Independent set, Clique, Digraph, Orientation, Strongly connected digraphs	1
1.7	Weekly connected digraphs, Unilaterally connected digraphs	1
1.8	Directed acyclic graph, Adjacency matrix, Incidence matrix of graphs, Trees, Spanning trees, Matrix tree theorem	1
1.9	Tutorial	2
2	**Graph algorithms**	
2.1	Search algorithms, Depth first search and breadth first search	2
2.2	Spanning tree algorithm	1
2.3	Kruskal's and Prim's shortest path algorithm	1
2.4	Dijkstra's and Floyd, Marshall	1
2.5	Tutorial	2
2.6	Matching, Perfect matching, Bipartite matching	1
2.7	Flow networks, Augmenting path algorithm	1
2.8	Min-cut and max-cut algorithms	1
2.9	Tutorial	2
3	**Linear Programming**	
3.1	Formulation of linear programming problem	1
3.2	Graphical method	2
3.3	Simplex method	1
3.4	Two phase method	1
3.5	Tutorial	2
3.6	Big M-method	1
3.7	Duality	1
3.8	Dual simplex method	1
3.9	Tutorial	2
4	**Integer and Dynamic Programming**	
4.1	Integer programming problem, Pure and mixed integer	1
4.2	Gomory's cutting plane algorithm	1
4.3	Dynamic programming problem, Principle of optimality	1
4.4	Backward and forward induction methods	1
4.5	Tutorial	2
4.6	Calculus method of solution, Tabular method of solution	2
4.7	Shortest path network problems	1
4.8	Applications in production	1
4.9	Tutorial	2
5	**Nontraditional Optimization Algorithms**	

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S. No	Topic	No. of Hours
5.1	Genetic Algorithm, Comparison between GA and traditional method	2
5.2	GA for constrained optimization	1
5.3	Ant colony optimization, Ant's foraging behavior and optimization	2
5.4	Tutorial	2
5.5	Artificial ants and minimum cost paths	1
5.6	Traveling salesman problem	1
5.7	ACO algorithm for traveling salesman problem	1
5.8	Tutorial	2
	Total	60

Course Designers

1. Mr. D.Senthil Raja -senthilrajad@ksrct.ac.in

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Department of ECE
K.S.Rangasamy College of Technology
Tiruchengode - 637 215.

60 PED 001	RESEARCH METHODOLOGY AND IPR	Category	L	T	P	Credit
		RM	3	0	0	3

Objective(s)

- To understand the principles of research process.
- To develop knowledge in analytical skills for collection of research data.
- To understand the procedure in the preparation of reports.
- To accomplish basic idea about the process involved in intellectual property rights.
- To enlighten the process of patent filing.

Pre-requisite

Nil

Course Outcomes

On the successful completion of the course, students will be able

CO1	To understand the research process and design.	Remember, Understand, Apply
CO2	To gain the knowledge about sources and collection of research data	Remember, Understand, Aanalyze
CO3	To understand the procedure of data analysis, preparation of reports and checking plagiarism	Remember, Understand, Analyze
CO4	To gain the knowledge on Trade mark and functions of UNESCO in IPR	Remember, Understand, Apply
CO5	To enlighten the benefits, E-filing and Examinations related to patents	Remember, Understand, Apply

Mapping with Programme Outcomes

COURSE NAME	CO	PO						PSO		
		1	2	3	4	5	6	1	2	3
Research Methodology and IPR	CO1	3	3	2	2	2	2	3	1	3
	CO2	3	3	2	2	2	2	3	1	3
	CO3	3	3	2	2	2	2	3	1	3
	CO4	3	3	2	2	2	2	3	1	3
	CO5	3	3	2	2	2	2	3	1	3

1-low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		Model Exam (Marks)	End Semester Examination (Marks)
	1	2		
Remember(Re)	10	10	20	30
Understand(Un)	20	20	40	30
Apply (Ap)	30	30	40	30
Analyze (An)	0	0	0	10
Evaluate(Ev)	0	0	0	0
Creative (Cr)	0	0	0	0
Total	60	60	100	100

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K.S.Rangasamy College of Technology – Autonomous R2022								
60 PED 001 - RESEARCH METHODOLOGY AND IPR								
Common to all Branches								
Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Research Design Overview of research process and design- Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys, Selection of the Right Medium and Journal for publication, Translation of Research	[9]
Data Collection and Sources Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.	[9]
Data Analysis and Reporting Overview of Multivariate Analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation. Checks for Plagiarism, Falsification, Fabrication, and Misrepresentation	[9]
Intellectual Property Rights Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.	[9]
Patents Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.	[9]
Total Hours	45

Text Book(s):

1.	David I. Bainbridge, “Intellectual Property”, Longman, 9th Edition, 2012.
2	Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education,

Reference(s):

1.	Chawla H S., “Introduction to Intellectual Property Rights”, CBS PUB & DIST PVT Limited, INDIA, 2019.
2.	Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007
3.	David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007
4.	Arun K. Narasani, Kankanala K.C., Radhakrishnan V., “Indian Patent Law and Practice”, Oxford University Press, 2010.
5.	Richard Stim, “Patent, Copyright & Trademark - An Intellectual Property Desk Reference”, NOLO Publishers, 2020.
6.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

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Course Content and Lecture Schedule

S.No.	Topics	No.of hours
1.0	**Research Design**	
1.1	Overview of research process and design	1
1.2	Use of Secondary and exploratory data to answer the research question	2
1.3	Qualitative research	1
1.4	Observation studies	1
1.5	Experiments and Surveys	1
1.6	Selection of the Right Medium and Journal for publication	2
1.7	Translation of Research	1
2.0	**Data Collection and Sources**	
2.1	Measurements, Measurement Scales	2
2.2	Questionnaires and Instruments	2
2.3	Sampling and methods	2
2.4	Data - Preparing, Exploring, examining and displaying	3
3.0	**Data Analysis and Reporting**	
3.1	Overview of Multivariate analysis	1
3.2	Hypotheses testing and Measures of Association	2
3.3	Presenting Insights	1
3.4	Findings using written reports and oral presentation	2
3.5	Checks for Plagiarism	1
3.6	Falsification	1
3.7	Fabrication, and Misrepresentation	1
4.0	**Intellectual Property Rights**	
4.1	Intellectual Property – The concept of IPR	1
4.2	Evolution and development of concept of IPR, IPR development process	2
4.3	Trade secrets, utility Models, IPR & Bio diversity	2
4.4	Role of WIPO and WTO in IPR establishments	1
4.5	Right of Property, Common rules of IPR practices	1
4.6	Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance	2
5.0	**Patents**	
5.1	Patents – objectives and benefits of patent, Concept, features of patent	2

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5.2	Inventive step, Specification, Types of patent application	2
5.3	Process E-filling, Examination of patent	1
5.4	Grant of patent, Revocation	1
5.5	Equitable Assignments, Licences, Licensing of related patents	2
5.6	Patent agents, Registration of patent agents	1

Course Designer

Dr.A.Murugesan – murugesana@ksrct.ac.in

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60 PVL 103	ANALOG IC DESIGN

Category	L	T	P	Credit
PC	3	0	0	3

Objective

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.
- To study the most important building blocks of all CMOS analog IC
- The basic principle of operation, the circuit choices and the trade-offs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.
- To know the band gap references and temperature independent references

Prerequisite

Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design amplifiers to meet user specifications	Apply
CO2	Analyze the frequency and noise performance of amplifiers	Analyze
CO3	Design and analyze feedback amplifiers and one stage op amps	Apply
CO4	Design and analyze two stage op amps	Apply
CO5	Design and analyze current mirrors and current sinks with mos devices	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	2	3
CO2	3	3	3	2	2	3
CO3	3	3	3	2	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	10	10	30
Understand(Un)	20	20	10
Apply (Ap)	20	20	30
Analyze (An)	10	10	15
Evaluate(Ev)	0	0	0
Creative (Cr)	10	10	15
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL 103 – ANALOG IC DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Note: Hours notified against each unit in the syllabus are only indicative but are not decisive. Faculty may decide the number of hours for each unit depending upon the concepts and depth. Questions need not be asked based on the number of hours notified against each unit in the syllabus

SINGLE STAGE AMPLIFIERS Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascade and Folded Cascade configurations with active load, design of Differential and Cascade Amplifiers - to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures	[9]
HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascade and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.	[9]
FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS Properties and types of negative feedback circuits, effect of loading in feedback networks, Operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.	[9]
STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER Analysis of Two Stage Op Amp - Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascade Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, and Compensation of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.	[9]
BANDGAP REFERENCES Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascade current source, design of high swing cascade sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing	[9]
Total hours	**45**

Text book(s):

1. Behzad Razavi, "Design Of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.

Reference(s):

1. Grebene, "Bipolar And Mos Analog Integrated Circuit Design", John Wiley & Sons, Inc.,2003.
2. Phillip E.Allen, Douglas R .Holberg, "Cmos Analog Circuit Design", Oxford University Press, 2nd Edition, 2002.
3. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320 2021/start
4. Jacob Baker "CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

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Course Content and Lecture Schedule

S. No	Topic	No. of Hours
1	**SINGLE STAGE AMPLIFIERS**	
1.1	Basic MOS physics and equivalent circuits and models	1
1.2	CS, CG and Source Follower	1
1.3	Differential amplifier with active load	1
1.4	Cascade and Folded Cascade configurations with active load	1
1.5	Design of Differential and Cascade Amplifiers	1
1.6	Slew Rate, noise, gain, Bandwidth	1
1.7	ICMR and power dissipation	1
1.8	Voltage swing	1
1.9	High gain amplifier structures	1
2	**HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS**	
2.1	Miller effect	1
2.2	Association of poles with nodes	1
2.3	Frequency response of CS, CG	1
2.4	Frequency response of Source Follower	1
2.5	Cascade Amplifier stages	1
2.6	Differential Amplifier stages	1
2.7	Statistical characteristics of noise	1
2.8	Noise in Single Stage amplifiers	1
2.9	Noise in Differential Amplifiers	1
3	**FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS**	
3.1	Properties and types of negative feedback circuits	1
3.2	Effect of loading in feedback networks	1
3.3	Operational amplifier performance parameters	1
3.4	Single stage Op Amps	1
3.5	Two stage Op Amps	1
3.6	Input range limitations and gain boosting	1
3.7	Slew rate, power supply rejection	1
3.8	Noise in Op Amps	1
4	**STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER**	
4.1	Analysis of Two Stage Op Amp	1
4.2	Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascade Second Stage	2
4.3	Multiple Systems	1
4.4	Phase Margin	1
4.5	Frequency Compensation	1
4.6	Compensation of Two Stage Op Amps	1
4.7	Slewing In Two Stage Op Amps	1
4.8	Other Compensation Techniques	1

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S. No	Topic	No. of Hours
5	**BANDGAP REFERENCES**	
5.1	Current sinks, sources and current mirrors	1
5.2	Wilson current source, Widlar current source	1
5.3	Cascade current source	1
5.4	Design of high swing cascade sink	1
5.5	Current amplifiers	1
5.6	Supply independent biasing	1
5.7	Temperature independent references	1
5.8	PTAT and CTAT current generation	1
5.9	Constant-gm biasing	1
	Total	45

Course Designers

1. Saravanan S - saravanan.s@ksrct.ac.in

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60 PVL 104	DIGITAL CMOS VLSI DESIGN

Category	L	T	P	Credit
PC	3	0	0	3

Objective

- To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit Tentative choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption
- To focus the CMOS data path design
- To describe the memory subsystems for CMOS circuits

Prerequisite

Digital logic design, VLSI Design

Course Outcomes

CO1	Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits	Understand, Apply, Analysis
CO2	Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort	Remember, Understand, Apply
CO3	Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches	Understand, Apply
CO4	Understand design methodology of arithmetic building blocks	Remember, Understand, Apply
CO5	Design functional units including ROM and SRAM	Remember, Understand, Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	15	15	30
Understand(Un)	15	10	20
Apply (Ap)	20	25	30
Analyze (An)	10	10	20
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL 104 – Digital CMOS VLSI design								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Note: Hours notified against each unit in the syllabus are only indicative but are not decisive. Faculty may decide the number of hours for each unit depending upon the concepts and depth. Questions need not be asked based on the number of hours notified against each unit in the syllabus

MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, Elmore constant, CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.	[10]
COMBINATIONAL LOGIC CIRCUITS Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates	[9]
SEQUENTIAL LOGIC CIRCUITS Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, non-bistable sequential circuits.	[9]
ARITHMETIC BUILDING BLOCKS Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.	[9]
MEMORY ARCHITECTURES Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.	[6]
Total hours	**45**

Text book(s):	
1.	N.Weste, K. Eshraghian, " Principles Of CMOS VLSI Design", Addision Wesley, 2nd Edition, 2018.
2.	Jan Rabaey, AnanthaChandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2018
Reference(s):	
1.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 2012
2.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 2019
3.	Jacob Baker "CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.
4.	Yuan Taur and TakH.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

Course Contents and Lecture Schedule

S.No	Topic	No.of Hours
1	**MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER**	
1.1	MOSFET characteristic under static and dynamic conditions	2
1.2	MOSFET secondary effects	2
1.3	Elmore constant	1
1.4	CMOS inverter-static characteristic	1
1.5	CMOS inverter-dynamic characteristic	1
1.6	Power, energy, and energy delay parameters	2
1.7	Stick diagram	1
1.8	Layout diagrams	2
2	**COMBINATIONAL LOGIC CIRCUITS**	

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2.1	Static CMOS design	1
2.2	Different styles of logic circuits	2
2.3	Logical effort of complex gates	1
2.4	Static and dynamic properties of complex gates	2
2.5	Interconnect delay	1
2.6	Dynamic logic gates	2
3	**SEQUENTIAL LOGIC CIRCUITS**	
3.1	Static latches and registers	2
3.2	Dynamic latches and registers	2
3.3	Timing issues	1
3.4	Pipelines	1
3.5	Clocking strategies	1
3.6	Non-bistable sequential circuits	2
4	**ARITHMETIC BUILDING BLOCKS**	
4.1	Data path circuits	2
4.2	Architectures for adders	2
4.3	Accumulators	1
4.4	Multipliers	1
4.5	Barrel shifters	2
4.6	Speed, power and area tradeoffs	1
5	**MEMORY ARCHITECTURES**	
5.1	Memory architectures and Memory control circuits	1
5.2	Read-Only Memories	1
5.3	ROM cells, Read Write Memories (RAM)	1
5.4	Dynamic memory design	1
5.5	6 Transistor SRAM cell	1
5.6	Sense amplifiers	1
	Total	45

Course Designers

1. Mrs.R.Ramya–rramya@ksrct.ac.in

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60 PVL 105	ADVANCED DIGITAL SYSTEM DESIGN

Category	L	T	P	Credit
PC	3	2	0	4

Objective

- To design asynchronous sequential circuits
- To analyse hazards in asynchronous sequential circuits,
- To study the fault testing procedure for digital circuits.
- To learn about the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

Prerequisite

Digital Logic Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design and analyze synchronous sequential circuits.	Remember, Understand
CO2	Analyze hazards in asynchronous sequential circuits.	Apply
CO3	Discuss the testing procedure for combinational circuit and PLA.	Apply, Analyse
CO4	Design PLD and ROM.	Apply, Analyse
CO5	Design and use programming tools for implementing digital circuits	Apply, Analyse

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	10	10	30
Understand (Un)	20	20	30
Apply (Ap)	30	30	30
Analyze (An)	0	0	10
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL 105- ADVANCED DIGITAL SYSTEM DESIGN								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
I	3	2	0	60	4	40	60	100

Note: Hours notified against each unit in the syllabus are only indicative but are not decisive. Faculty may decide the number of hours for each unit depending upon the concepts and depth. Questions need not be asked based on the number of hours notified against each unit in the syllabus

Sequential Circuit Design Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart	[12]
Asynchronous Sequential Circuit Design Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment- Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.	[12]
Fault Diagnosis and Testability Algorithms Fault Table Method-Path Sensitization Method – Boolean Difference Method - Kohavi Algorithm D Algorithm —Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test	[12]
Synchronous Design Using Programmable Devices and System Design Using VHDL Programmable Logic Devices – Designing a Synchronous Sequential Circuit using PLA/ PAL Computer Aided Design – Realization of Finite State Machine using PLD.FPGA – Xilinx FPGA - Xilinx 2000 - Xilinx 3000 - Xilinx 4000. VHDL Description of Combinational Circuits and sequential circuit. VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL	[12]
Timing Analysis ROM timings - Static RAM timing - Synchronous Static RAM and it's timing - Dynamic RAM timing, Complex Programmable Logic Devices - Logic Analyzer Basic Architecture - Internal structure - Data display - Setup and Control - Clocking and Sampling	[12]
Total hours	**60**

Text book(s):

1. Donald G. Givone, 'Digital principles and Design', Tata McGraw Hill, 2016.
2. John M Yarbrough, 'Digital Logic applications and Design', Thomson Learning, 2017.

Reference(s):

1. Nripendra N Biswas, 'Logic Design Theory', Prentice Hall of India Private Ltd., 2016.
2. Charles H. Roth Jr., 'Digital System Design using VHDL', Thomson Learning, 2016.
3. J.F.Wakerly, 'Digital Design Principles and Practices', 4th Edition, Pearson Education, 2017.
4. J.F.Wakerly, 'Digital Design: Principles and Practices', 3rd Edition, Pearson Education, 2016.

Course Contents and Lecture Schedule

S. No	Topic	No.of Hours
1	**Sequential Circuit Design**	
1.1	Analysis of Clocked Synchronous Sequential Circuits and Modelling	2
1.2	State Diagram	1
1.3	State Table, State Table Assignment and Reduction	2
1.4	Design of Synchronous Sequential Circuits	2
1.5	Design of Iterative Circuits	2
1.6	ASM Chart	2
2	**Asynchronous Sequential Circuit Design**	

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2.1	Analysis of Asynchronous Sequential Circuit	2
2.2	Flow Table Reduction	2
2.3	Races-State Assignment	1
2.4	Transition Table and Problems in Transition Table.	1
2.5	Design of Asynchronous Sequential	1
2.6	Circuit - Static, Dynamic and Essential	2
2.7	hazards	1
2.8	Mixed Operating Mode Asynchronous Circuits	1
2.9	Designing Vending Machine Controller	1
3	**Fault Diagnosis and Testability Algorithms**	
3.1	Fault Table Method	1
3.2	Path Sensitization Method	1
3.3	Boolean Difference Method	2
3.4	Kohavi Algorithm D Algorithm	2
3.5	Tolerance Techniques	2
3.6	The Compact Algorithm	1
3.7	Fault in PLA	1
3.8	Test Generation	1
3.9	DFT Schemes – Built in Self Test	1
4	**Synchronous Design Using Programmable Devices and System Design Using VHDL**	
4.1	Programmable Logic Devices	1
4.2	Designing a Synchronous Sequential Circuit using PLA/ PAL Computer Aided Design	2
4.3	Realization of Finite State Machine using PLD.FPGA	1
4.4	Xilinx FPGA	1
4.5	Xilinx 2000 - Xilinx 3000 - Xilinx 4000.	1
4.6	VHDL Description of Combinational Circuits and sequential circuit.	2
4.7	VHDL Operators	2
4.8	Compilation and Simulation of VHDL Code – Modeling using VHDL	2
5	**Timing Analysis**	
5.1	ROM timings	2
5.2	Static RAM timing	2
5.3	Synchronous Static RAM and it's timing	2
5.4	Dynamic RAM timing	1
5.5	Complex Programmable Logic Devices	1
5.6	Logic Analyzer Basic Architecture	1
5.7	Internal structure	1
5.8	Data display	1
5.9	Setup and Control - Clocking and Sampling	1

Course Designers

1. Dr.S.MALARKHODI - malarkhodi@ksrct.ac.in

60 PVL 106		**Category**	**L**	**T**	**P**	**Credit**

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	ADVANCED EMBEDDED COMPUTING	PC	3	0	0	3

Objective

- To impart the knowledge of the Embedded design
- To learn and apply embedded networks in different application
- To study the design methodologies of an embedded system
- To know the basics of embedded product design
- To introduce the embedded product lifecycle

Prerequisite

Embedded Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquire knowledge of embedded system design	Remember, Understand
CO2	Describe the embedded network systems and architectures	Remember, Understand
CO3	Describe the Embedded system with different system design techniques	Remember, Apply
CO4	Design and develop an embedded product	Analyse, Apply
CO5	Develop the product life cycle of an electronic product	Analyse, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			
CO2	3		3			
CO3	3	3	3	3	3	
CO4	3	3	3	3	3	2
CO5	3	3	3	3	3	
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	20	10	30
Understand (Un)	20	20	30
Apply (Ap)	20	20	30
Analyze (An)	0	10	10
Evaluate (Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL 106 - ADVANCED EMBEDDED COMPUTING								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Note: Hours notified against each unit in the syllabus are only indicative but are not decisive. Faculty may decide the number of hours for each unit depending upon the concepts and depth. Questions need not be asked based on the number of hours notified against each unit in the syllabus

Structure of Embedded Systems Core – Memory – Sensors and Actuators – Communication Interface – Embedded Firmware – Other system components – Characteristics and Quality Attributes of Embedded System	[9]
Networks Distributed Embedded Architectures - Networks for Embedded Systems - Network Based Design - Internet-Enabled Systems - Vehicles as Networks - Sensor Networks	[9]
System Design Techniques Design Methodologies - Requirements Analysis – Specifications - System Analysis and Architecture Design - Quality Assurance – Hardware software co-design and program modelling	[9]
Design and Development of Embedded Product Embedded Hardware Design and Development – Embedded Firmware Development – Integration and testing of Embedded hardware and firmware – Embedded system development environment	[9]
Embedded product development Life Cycle Introduction to EDLC – Objectives – different phases of EDLC – ELDC Approaches – Processor trends – Embedded OS Trends – Development language Trends – Open standards, framework and alliances – Bottlenecks	[9]
Total hours	**45**

Text book(s):	
1.	Introduction to Embedded Systems by Shibu K.V.,Tata Mcgraw Hill Education (India) Private Limited, 2009
2.	Computers as Components - Principles of Embedded Computing System Design by Wayne Wolf, Second Edition, Elsevier.
Reference(s):	
1.	Embedded system-Architecture, Programming, Design by Rajkamal, TMH,2011.
2.	Embedded Systems-An Integrated Approach by Lyla B Das ,Pearson, 2013

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Structure of Embedded Systems**	
1.1	Core	1
1.2	Memory	1
1.3	Sensors and Actuators	1
1.4	Communication Interface	2
1.5	Embedded Firmware	1
1.6	Other system components	1
1.7	Characteristics and Quality Attributes of Embedded System	2
2	**Networks**	

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2.1	Distributed Embedded Architectures	2
2.2	Networks for Embedded Systems	2
2.3	Network Based Design	2
2.4	Internet-Enabled Systems	1
2.5	Vehicles as Networks	1
2.6	Sensor Networks	1
3	**System Design Techniques**	
3.1	Design Methodologies	2
3.2	Requirements Analysis	1
3.3	Specifications	1
3.4	System Analysis and Architecture Design	2
3.5	Quality Assurance	1
3.6	Hardware software co-design and program modelling	1
4	**Design and Development of Embedded Product**	
4.1	Embedded Hardware Design and Development	3
4.2	Embedded Firmware Development	2
4.3	Integration and testing of Embedded hardware and firmware	2
4.4	Embedded system development environment	2
5	**Embedded product development Life Cycle**	
5.1	Introduction to EDLC	1
5.2	Objectives	1
5.3	Different phases of EDLC	1
5.4	ELDC Approaches	1
5.5	Processor trends	1
5.6	Embedded OS Trends	1
5.7	Development language Trends	1
5.8	Open standards, framework and alliances	1
5.9	Bottlenecks	1
	Total	45

Course Designers

1. Dr.C.Rajasekaran – rajasekaran@ksrct.ac.in
2. Mr.K.Raguvaran – raguvaran@ksrct.ac.in

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60 PVL 1P1	VLSI Laboratory I

Category	L	T	P	Credit
PC	0	0	4	2

Objective

- To help the engineers to design the system with Verilog Hardware Description Language
- To practice for writing synthesizable RTL models that work correctly in both simulation and synthesis with FPGA.
- To design various VLSI subsystem using Verilog Hardware Description Language
- To develop prototype systems using FPGA.
- To analyse all important issues related to size, speed and power consumption using VLSI EDA tools

Prerequisite

Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Use EDA tool to design complex combinational and sequential circuits	Create
CO2	Design sequential circuits using Verilog HDL	Create
CO3	Analyse various adder & multiplier subsystem using Verilog HDL	Analyse, Create
CO4	Demonstrate FPGA implementation of various digital logic circuits	Create
CO5	Develop and prototype digital systems design using FPGA	Create

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1- low, 2- medium, 3- high

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60 PVL 1P1 – VLSI Laboratory I

M.E-VLSI Design

Semester	Hours / Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

1. Design and verification of Combinational Circuits using Verilog HDL
2. Design and verification of Sequential Circuits using Verilog HDL
3. Design, simulate and synthesis of Finite State Machine using Verilog HDL
4. Design of Low Power, High Speed VLSI Adder Subsystems
5. Design of Low Power, High Speed VLSI Multiplier Subsystems
6. Design of Low power filter using Verilog HDL
7. Implement ALU using FPGA
8. Implement Image processing algorithm on FPGA through system generator
9. Implement smart home system using FPGA
10. Implement Health Monitoring System using FPGA

Course Designers

1. Mrs.C.Saranya – saranyac@ksrct.ac.in

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60 PVL 1P2	ANALOG IC DESIGN LABOROTARY

Category	L	T	P	Credit
PC	0	0	4	2

Objective

- Carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed
- To bring out the key aspects of each important module in the CAD tool including the simulation
- To design differential amplifier and analyze the performance
- To design layout, LVS and parasitic extracted simulation using CAD tools

Prerequisite

Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design digital and analog circuit using CMOS given a design specification.	Apply
CO2	Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances	Apply
CO3	Develop layout for the CMOS circuit	Apply
CO4	Analyze the performance of different amplifiers	Apply
CO5	Use EDA tools for Circuit Design	Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	3
CO2	3	3	3	3	2	3
CO3	3	3	3	3	2	3
CO4	3	3	3	3	2	3
CO5	3	3	3	3	2	3

1- low, 2- medium, 3- high

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60 PVL 1P2–ANALOG IC DESIGN LABORATORY								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

1. Extraction of process parameters of CMOS process transistors
   a. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b. Plot I_D vs. V_{GS} at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log I_D vs. V_{GS} at particular gate voltage for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.
   d. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage To extract V_{th} use the following procedure.
      i. Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
      ii. Plot y= I_D/(g_m) as a function of V_{GS} using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   f. Plot Io vs. Vos at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.

2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in}, and determine transition voltage and gain g. Calculate V_{IL}, V_{IH}, NM_H, NM_L for the inverter.
      ii. Plot VTC for CMOS inverter with varying V_{DD}.
      iii. Plot VTC for CMOS inverter with varying device ratio.

b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay t_{pHL}, t_{pLH}, 20%-to-80% rise time t_r and 80%-to-20% fall time t_f.

c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve VDSQ=VDD/2.
      ii. Calculate input bias voltage for a given bias current.
      iii. Use spice and obtain the bias current. Compare with the theoretical value
      iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
      v. using small signal analysis in spice, considering load capacitance.
      vi. Plot step response of the amplifier with a specific input pulse amplitude.
      vii. Derive time constant of the output and compare it with the time constant resulted from -3dB Band Width.
      viii. Use spice to determine input voltage range of the amplifier

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5. Three OPAMP Instrumentation Amplifier (INA).
   Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
   i. Draw the schematic of op-amp macro model.
   ii. Draw the schematic of INA.
   iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
      i. low-frequency voltage gain,
      ii. unity gain BW (fu),
      iii. input capacitance,
      iv. output resistance,
      v. CMRR
   iv. Draw schematic diagram of CMRR simulation setup.
   v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
   vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
   vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.
   a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal-1 as interconnect line between inverters.
   b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
   c. Extract the netlist. Use extracted netlist and obtain t_{pHL}, t_{pLH} for the inverter using Spice.
   d. Use a specific interconnect length and connect and connect three inverters in a chain.
   e. Extract the new netlist and obtain teat and tee of the middle inverter.
   f. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
      a. low-frequency voltage gain,
      b. unity gain BW (fu),
      c. Power dissipation
   i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
   ii. Perform time domain simulation and verify low frequency gain.
   iii. Perform AC analysis and verify.

Course Designers

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60 PVL 201	DESIGN AND VERIFICATION USING UVM

Category	L	T	P	Credit
PC	3	0	0	3

Objective

This course aims

- To provide the students, a complete understanding on UVM testing
- To become proficient at UVM verification
- To Know about the verification components used and to build it
- To describe the register layer classes and to generate it
- To learn all peripheral bus test benches and its advanced level

Prerequisite

System Verilog

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the basic concepts of two methodologies UVM	Remember, Understand
CO2	Build actual verification components	Apply
CO3	Generate the register layer classes	Apply
CO4	Code test benches using UVM	Apply
CO5	Understand advanced peripheral bus test benches	Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3		3
CO2	3		3	3		3
CO3	3		3	3		3
CO4	3		3	3		3
CO5	3		3	3		3
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	10	10	30
Understand(Un)	20	20	30
Apply (Ap)	30	30	30
Analyze (An)	0	0	10
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology–Autonomous R2022								
60 PVL 201 – DESIGN FOR VERIFICATION USING UVM								
M.E-VLSI Design								
Semester	Hours/Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation	[9]
Developing Reusable Verification Components Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver – Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test- Implementing Checks and Coverage	[9]
UVM using Verification Components Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test – Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model	[9]
UVM using the Register Layer Classes Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- PreDefined Sequences	[9]
Assignment in Test benches Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.	[9]
Total Hours	45

Text Book(s):	
1.	https://www.accellera.org/images/downloads/standards/uvm/uvm_users_guide_1.1.pdf
2.	https://www.udemy.com/course/learn-ovm-uvm/
Reference(s):	
1.	http://www.testbench.in/ot_00_index.html
2.	http://www.testbench.in/UT_00_INDEX.html

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Introduction to UVM**	
1.1	Overview	1
1.2	Typical UVM Testbench Architecture	1
1.3	UVM Class Library	1
1.4	Transaction-Level Modeling - Overview	1
1.5	TLM, TLM-1	2
1.6	TLM-2.0	1
1.7	TLM-1 Implementation	1
1.8	TLM-2.0 Implementation	1
2	**Developing Reusable Verification Components**	

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S.No	Topic	No. of Hours
2.1	Modeling Data Items for Generation	1
2.2	Transaction-Level Components	1
2.3	Creating the Driver	1
2.4	Creating the Sequencer	1
2.5	Connecting the Driver and Sequencer, Creating the Monitor	1
2.6	Instantiating Components, Creating the Agent	1
2.7	Creating the Environment	1
2.8	Enabling Scenario Creation	1
2.9	Managing of Test-Implementing Checks and Coverage	1
3	**UVM USING VERIFICATION COMPONENTS**	
3.1	Creating a Top-Level Environment	1
3.2	Instantiating Verification Components	1
3.3	Creating Test Classes	1
3.4	Verification Component Configuration	1
3.5	Creating and Selecting a User-Defined Test	1
3.6	Creating Meaningful Tests- Virtual Sequences	1
3.7	Checking for DUT Correctness	1
3.8	Scoreboards	1
3.9	Implementing a Coverage Model	1
4	**UVM using the Register Layer Classes**	
4.1	Using The Register Layer Classes	1
4.2	Back-Door Access	1
4.3	Special Registers	1
4.4	Integrating a Register Model in a Verification Environment	2
4.5	Integrating a Register Model	2
4.6	Randomizing Field Values	1
4.7	PreDefined Sequences	1
5	**Assignment in Test benches**	
5.1	Assignment	1
5.2	APB: Protocol	1
5.3	Test bench Architecture	1
5.4	Driver and Sequencer	1
5.5	Monitor, Agent and Env	1
5.6	Creating Sequences	1
5.7	Building Test	1
5.8	Design and Testing of Top Module	2
	Total	**45**

Course Designers

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60 PVL 202	LOW POWER VLSI DESIGN

Category	L	T	P	Credit

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		PC	3	0	0	3

Objective

- To identify sources of power in an IC
- To identify the power reduction techniques based on technology independent and technology dependent methods
- To identify suitable techniques to reduce the power dissipation
- To estimate power dissipation of various MOS logic circuits
- To develop algorithms for low power dissipation

Prerequisite

Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Find the power dissipation of MOS circuits	Remember, Understand
CO2	Design and analyze various MOS logic circuits	Remember, Understand
CO3	Apply low power techniques for low power dissipation	Remember, Apply, Analyse
CO4	Estimate the power dissipation of ICs	Remember, Apply
CO5	Develop algorithms to reduce power dissipation by software	Remember, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3			3
CO2	3		3	2		3
CO3			3			3
CO4			3			3
CO5	3		3	3		3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	15	15	30
Understand (Un)	10	10	20
Apply (Ap)	20	20	30
Analyze (An)	15	15	20
Evaluate (Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL 202 – LOW POWER VLSI DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

POWER DISSIPATION IN CMOS Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.	[9]
POWER OPTIMIZATION Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design– Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design	[9]
DESIGN OF LOW POWER CMOS CIRCUITS Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption In Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques –Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.	[9]
POWER ESTIMATION Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, –Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis	[9]
SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWERCMOS CIRCUITS Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.	[9]
Total hours	**45**

Text book(s):	
1.	Kaushik Roy and S.C.Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2000
2.	J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 1999.
Reference(s):	
1.	James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001
2.	J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009
3.	David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, “Low Power Methodology Manual: For System-on-Chip Design (Integrated Circuits and Systems) ” Springer, 2008.
4.	Yuan Taur and TakH.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

Course Contents and Lecture Schedule

S. No	Topic	No. of Hours
1	**POWER DISSIPATION IN CMOS**	
1.1	Hierarchy of Limits of Power	2
1.2	Sources of Power Consumption	3
1.3	Physics of Power Dissipation in CMOS FET Devices	3
1.4	Basic Principle of Low Power Design	1
2	**POWER OPTIMIZATION**	
2.1	Logic Level Power Optimization	2
2.2	Circuit Level Low Power Design	2
2.3	Gate Level Low Power Design	1
2.4	Architecture Level Low Power Design	2
2.5	VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design	2
3	**DESIGN OF LOW POWER CMOS CIRCUITS**	
3.1	Computer Arithmetic Techniques for Low Power System	1

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3.2	Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories	2
3.3	Low Power Clock	2
3.4	Advanced Techniques	1
3.5	Special Techniques, Adiabatic Techniques	2
3.6	Physical Design, Floor Planning, Placement and Routing	1
4	**POWER ESTIMATION**	
4.1	Power Estimation Techniques	1
4.2	Circuit Level, Gate Level	2
4.3	Architecture Level, Behavioral Level	2
4.4	Logic Power Estimation	2
4.5	Simulation Power Analysis	1
4.6	Probabilistic Power Analysis	1
5	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS**	
5.1	Synthesis for Low Power	2
5.2	Behavioral Level Transform	3
5.3	Algorithms for Low Power	2
5.4	Software Design for Low Power	2
	Total	45

Course Designers

1. Mrs.C.Saranya–saranyac@ksrct.ac.in

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60 PVL 203	RF CIRCUIT DESIGN

Category	L	T	P	Credit
PC	3	0	0	3

Objective

- To introduce the principles of operation and design principles of important blocks like Low Noise Amplifiers
- To study the concepts of Phase Locked Loop Synthesizers
- To study the feedback systems and types of amplifiers
- To learn the concepts of Mixers and Oscillators
- To learn impedance matching circuits in RF domain

Prerequisite

RF Passive and Active Devices, Transmission Lines.

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the basic principles of MOSFET physics, transceiver specifications and Architectures.	Remember, Understand Apply
CO2	Discuss the principle of impedance matching and amplifiers	Remember, Understand Apply
CO3	Describe the working principle of feedback systems and power amplifiers	Understand Apply
CO4	Explain the configuration of RF filter design, mixers and oscillators	Understand Analyze
CO5	Describe the concepts of PLL and Frequency Synthesizers.	Remember, Understand Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	3			
CO2	3	3	3	3	
CO3	3	3	3	3	
CO4	3	3	3	3	2
CO5	3				2

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	10	10	20
Understand (Un)	15	15	30
Apply (Ap)	20	20	30
Analyze (An)	15	15	20
Evaluate (Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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60 PVL 203- RF CIRCUIT DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

CMOS Physics- Transceiver Specifications and Architectures Introduction to MOSFET Physics- Noise - Thermal- shot- flicker- popcorn noise - Two port Noise theory - Noise Figure – THD - IP2 - IP3 – Sensitivity – SFDR - Phase noise - Specification distribution over a communication link - Homodyne Receiver - Heterodyne Receiver - Image reject - Low IF Receiver Architectures Direct up conversion Transmitter - Two step up conversion Transmitter.	[9]
Impedance Matching and Amplifiers S -parameters with Smith chart - Passive IC components - Impedance matching networks - Common Gate - Common Source Amplifiers - OC Time constants in bandwidth estimation and enhancement - High frequency amplifier design - Power match and Noise match - Single ended and Differential LNAs - Terminated with Resistors and Source Degeneration LNAs.	[9]
Feedback Systems and Power Amplifiers Stability of feedback systems: Gain and phase margin - Root -locus techniques - Time and Frequency domain considerations - Compensation - General model – Class A, AB, B C, D, E and F amplifiers - Power amplifier Linearization Techniques - Efficiency boosting techniques - ACPR metric - Design Considerations.	[9]
RF Filter Design, Oscillator and Mixer Overview-basic resonator and filter configuration-special filter realizations-filter implementation. Basic oscillator model-high frequency oscillator configuration- basic characteristics of mixers-phase locked loops-RF directional couplers hybrid couplers-detector and demodulator circuits.	[9]
PLL and Frequency Synthesizers Linearized Model - Noise properties - Phase detectors - Loop filters and Charge pumps - Integer -N frequency synthesizers - Direct Digital Frequency synthesizers.	[9]
Total hours	**45**

Text book(s):	
1.	LEE, T.H.Lee, 'Design of CMOS RF Integrated Circuits', Cambridge University Press, 2013.
2.	B.Razavi, 'RF Microelectronics', 2nd Edition, Pearson Education, 2013.
Reference(s):	
1.	Jan Crols, MichielSteyaert, 'CMOS Wireless Transceiver Design', Springer, 2010.
2.	B.Razavi, 'Design of Analog CMOS Integrated Circuits', Tata McGraw-Hill, 2012.
3.	Matthew M.Radmanesh,' Radio frequency and Microwave Electronics illustrated', Pearson Education Inc, Delhi, 2006.
4.	Recorded lectures and notes available at. http://www.ee.iitm.ac.in/~ani/ee6240/

Course Contents and Lecture Schedule

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S.No	Topic	No. of Hours
1	**CMOS PHYSICS- TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES**	
1.1	Introduction to MOSFET Physics	1
1.2	Noise - Thermal- shot- flicker- popcorn noise	2
1.3	Two port Noise theory - Noise Figure – THD - IP2 - IP3 – Sensitivity	2
1.4	SFDR - Phase noise - Specification distribution over a communication link - Homodyne Receiver - Heterodyne Receiver	2
1.5	Image reject - Low IF Receiver Architectures Direct up conversion Transmitter - Two step up conversion Transmitter	2
2	**IMPEDANCE MATCHING AND AMPLIFIERS**	
2.1	S -parameters with Smith chart - Passive IC components	1
2.2	Impedance matching networks - Common Gate - Common Source Amplifiers	2
2.3	OC Time constants in bandwidth estimation and enhancement - High frequency amplifier design	2
2.4	Power match and Noise match - Single ended and Differential LNAs	2
2.5	Terminated with Resistors and Source Degeneration LNAs.	2
3	**FEEDBACK SYSTEMS AND POWER AMPLIFIERS**	
3.1	Stability of feedback systems: Gain and phase margin	1
3.2	Root -locus techniques - Time and Frequency domain considerations - Compensation	2
3.3	General model – Class A, AB, B C, D, E and F amplifiers	2
3.4	Power amplifier Linearization Techniques	2
3.5	Efficiency boosting techniques - ACPR metric - Design Considerations.	2
4	**RF FILTER DESIGN, OSCILLATOR AND MIXER**	
4.1	Overview-basic resonator and filter configuration	1
4.2	Special filter realizations-filter implementation. Basic oscillator model	2
4.3	high frequency oscillator configuration- basic characteristics of mixers	2
4.4	phase locked loops-RF directional couplers hybrid couplers	2
4.5	Detector and demodulator circuits.	2
5	**PLL AND FREQUENCY SYNTHESIZERS**	
5.1	Linearized Model - Noise properties	2
5.2	Phase detectors	2
5.3	Loop filters and Charge pumps	2
5.4	Integer -N frequency synthesizers	1
5.5	Direct Digital Frequency synthesizers.	2
	Total	45

Course Designers

1. Mr.R.Satheeshkumar–satheeshkumar@ksrct.ac.in

60 PVL 204	VLSI TESTING

Category	L	T	P	Credit

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		PC	3	0	0	3

Objective

- To introduce the VLSI testing.
- To introduce logic and fault simulation and testability measures
- To study the test generation for combinational and sequential circuits
- To study the design for testability.
- To study the fault diagnosis

Prerequisite

Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand VLSI Testing Process	Remember, Understand
CO2	Develop Logic Simulation and Fault Simulation	Remember, Understand
CO3	Develop Test for Combinational and Sequential Circuits	Understand, Apply, Analyse
CO4	Understand the Design for Testability	Remember, Understand Apply
CO5	Perform Fault Diagnosis	Understand Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3			3
CO2			3			3
CO3	3		3	3		3
CO4	3		3	3		3
CO5			3	2		3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	15	15	30
Understand (Un)	10	10	10
Apply (Ap)	25	25	50
Analyze (An)	10	10	10
Evaluate (Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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60 PVL 204- VLSI TESTING								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

INTRODUCTION TO TESTING Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing – Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.	[9]
LOGIC & FAULT SIMULATION & TESTABILITY MEASURES Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – SCOAP Controllability and Observability.	[9]
TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.	[9]
DESIGN FOR TESTABILITY Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built In Self-Test – Random Logic BIST – DFT for Other Test Objectives.	[9]
FAULT DIAGNOSIS Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.	[9]
Total hours	**45**

Text book(s):	
1.	Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017
2.	Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits" , Kluwer Academic Publishers, 2017
Reference(s):	
1.	Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press, 2017.
2.	N. K. Jha and S. Gupta ,"Testing of Digital Systems", Cambridge University Press, 2012
3.	Wang ,"VLSI Test Principles and Architectures: Design for Testability", Elsevier,2011
4.	ZeljkoZilic "Verification by Error Modeling: Using Testing Techniques in Hardware Verification", Springer,2010

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**INTRODUCTION TO TESTING**	
1.1	Introduction	1
1.2	VLSI Testing Process and Test Equipment	2
1.3	Challenges in VLSI Testing	1
1.4	Test Economics and Product Quality	1
1.5	Fault Modeling	2
1.6	Relationship Among Fault Models	2
2	**LOGIC & FAULT SIMULATION & TESTABILITY MEASURES**	
2.1	Simulation for Design Verification and Test Evaluation	2
2.2	Modeling Circuits for Simulation	2
2.3	Algorithms for True Value and Fault Simulation	2
2.4	SCOAP Controllability and Observability	3
3		
3.1	Algorithms and Representations	1

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3.2	Redundancy Identification	1
3.3	Combinational ATPG Algorithms	2
3.4	Sequential ATPG Algorithms	1
3.5	Simulation Based ATPG	2
3.6	Genetic Algorithm Based ATPG	2
4	**DESIGN FOR TESTABILITY**	
4.1	Design for Testability Basics	1
4.2	Testability Analysis	1
4.3	Scan Cell Designs	1
4.4	Scan Architecture	2
4.5	Built In Self-Test	1
4.6	Random Logic BIST	1
4.7	DFT for Other Test Objectives	2
5	**FAULT DIAGNOSIS**	
5.1	Introduction and Basic Definitions	1
5.2	Fault Models for Diagnosis	2
5.3	Generation of Vectors for Diagnosis	2
5.4	Combinational Logic Diagnosis	2
5.5	Scan Chain Diagnosis	1
5.6	Logic BIST Diagnosis	1
	Total	45

Course Designers

1. Mrs.C.Saranya–saranyac@ksrct.ac.in

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60 PVL 2P1	VLSI LABORATORY II

Category	L	T	P	Credit
PC	0	0	4	2

Objective

- To learn the concept of System Verilog HDL
- To help engineers understand, and maintain digital hardware models and conventional verification test benches written in System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog
- To develop Verilog test environments using EDA tools
- To learn the features and capabilities of the UVM class library for system Verilog

Prerequisite

Basic Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Use the System Verilog, to design and synthesis features of digital circuits	Create
CO2	Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.	Create
CO3	Implement higher level of abstraction to design and verification	Create
CO4	Develop Verilog test environments of significant capability and complexity	Create
CO5	Integrate scoreboards, multichannel sequencers and Register Models	Create

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1- low, 2- medium, 3- high

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60 PVL 2P1 – VLSI Laboratory II								
M.E-VLSI Design								
Semester	Hours / Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	0	0	4	60	2	60	40	100

1. Introduction to System Verilog and UVM
2. Modeling Combinational circuits using System Verilog
3. Design FIFO using system Verilog
4. Design on FSM using system Verilog
5. Use an interface between testbench and DUT
6. Developing a test program using system Verilog
7. Create a scoreboard using dynamic array
8. Use mailboxes for verification
9. Generate constrained random test values
10. Using coverage with constrained random tests

Total Hours:60

Course Designers

1. Mr.S.Saravanan – saravanan.s@ksrct.ac.in

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60 PVL 2P2	TERM PAPER AND SEMINAR

Category	L	T	P	Credit
PC	0	0	2	0

Objective

- Students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles.
- A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas.
- To identify the recent topics in the research area and formulate the problem
- To analyze the mathematical model for the identified problem
- To design and simulate/ develop prototype model

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Survey the relevant bibliography such as national/international referred journals for the preferred areas of research	Analyse
CO2	Develop scientific, technical reading and writing skills for the technical report preparation to apply it in their topics of research	Apply
CO3	Apply mathematical ideas to any problem in the research field	Apply
CO4	Implement and analyze the various complex problems in different practical applications	Analyse
CO5	Cultivate presentation skills to deliver their work in front of technically qualified audience	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	3	
CO2	3	3	3	2	3	3
CO3	3		3	3		3
CO4	3	2	3	3	2	3
CO5	3	3	3	2	3	
1- low, 2- medium, 3- high						

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60 PVL 2P2- TERM PAPER AND SEMINAR								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
II	0	0	2	30	0	100	00	100

The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic.
2. Stating an objective.
3. Collecting the relevant bibliography (at least 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline.
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

Activities to be carried out

Activity	**Instructions**	**Submission week**	**Evaluation**
Selection of area of interest and Topic Stating an Objective	An area of interest, topic has to be selected and objective to be framed	2nd week	**3%** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about chosen area & topic	The following details related to the chosen area must be collected. 1. List 1 special interest groups or professional 2. society 3. List 2 journals 4. List 3 conferences, symposia or workshops 5. List1+ thesis title 6. List 5 web presences (mailing lists, forums, 7. news sites) 8. List 6 authors who publish regularly in 9. your area 10. Attach a call for papers (CFP) from 11. Conference/Journal/Symposium in the chosen area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• Provide a complete list of references you will be using- Based on the objective - Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some way and/or that are in the same field so that a meaningful survey can be Written	4th week	**6%** (the list of standard papers and reason for selection)

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	• Favour papers from well-known journals and conferences, • Favour 'first' or 'foundational' papers in the field (as indicated in other people's survey paper), Favour more recent papers, • Pick a recent survey of the field to quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the • paper are being considered		
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? • Conclude with limitations/issues not addressed by the paper (from the • perspective of your survey)	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your
Draft outline 1 and Linking papers	Prepare a draft Outline, with survey goals, along with a classification / categorization Diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a Presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce

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Introduction Background	Write an introduction and background Sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of the paper chosen based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write conclusions and future work	12th week	**5%** (conclusions– clarity and your ideas)
Final Draft	Complete the final draft of the paper prepared	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on the paper prepared	14th& 15th week	**10%** (based on presentation and Viva-voce)

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60 PVL E11	NANO ELECTRONICS

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To learn basic concepts of Nano electronics.
- To know the techniques of fabrication and measurement.
- To study the properties of nanoelectronic materials
- To gain knowledge about Nanostructure devices.
- To know logic devices and applications

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the fundamentals of nanoelectronics	Remember, Understand
CO2	Describe the fabrication and measurement techniques of various nanostructures and nanotubes	Apply
CO3	Explain the properties of nanoelectronic materials	Apply
CO4	Know the various nanostructure devices	Remember, Understand
CO5	Describe the types of logic device and their applications	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	2	1
CO2	3	3	3	2	2	1
CO3	3	3	3	2	2	1
CO4	3	3	3	2	2	1
CO5	3	3	3	2	2	1

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	30	30	30
Understand(Un)	10	10	30
Apply (Ap)	20	20	40
Analyze (An)	0	0	0
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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60 PVL E11- NANO ELECTRONICS								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction to Nanoelectronics Microelectronics towards biomolecule electronics-Particles and waves- Wave-particle duality- Wave mechanics- Schrodinger wave equation- Wave mechanics of particles: Atoms and atomic orbitals- Materials for nanoelectronics- Semiconductors- Crystal lattices: Bonding in crystals- Electron energy bands- Semiconductor heterostructures- Lattice-matched and pseudomorphic heterostructures- Inorganic-organic heterostructures- Carbon nanomaterials: nanotubes and fullerenes.	[9]
Fabrication and Measurement Techniques Growth- fabrication- and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography- etching- and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems.	[9]
Properties Dielectrics-Ferroelectrics-Electronic Properties and Quantum Effects-Magneto electronics – Magnetism and Magneto transport in Layered Structures-Organic Molecules – Electronic Structures- Properties- and Reactions-Neurons – The Molecular Basis of their Electrical Excitability-Circuit and System Design- Analysis by Diffraction and Fluorescence Methods-Scanning Probe Techniques.	[9]
Nano Structure Devices Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots- Nanostructure devices- Resonant-tunneling diodes- Field-effect transistors- Single-electron-transfer devices- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Quantum-dot cellular automata.	[9]
Logic Devices and Applications Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing- Molecular Electronics.	[9]
	Total hours: 45

Reference(s):

1.	Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, 'Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications', Cambridge University Press, 2013.
2.	SupriyoDatta, 'Lessons from Nanoelectronics: A New Perspective on Transport', World Scientific, 2012.
3.	George W. Hanson, 'Fundamentals of Nanoelectronics', Pearson Education, 2012.
4.	Korkin, Anatoli; Rosei, Federico (Eds.), 'Nanoelectronics and Photonics', Springer, 2013.
5.	Mircea Dragoman, Daniela Dragoman, 'Nanoelectronics: Principles and Devices', CRC Press, 2012.
6.	Karl Goser, Peter Glosekotter, Jan Dienstuhl, 'Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices', Springer, 2013.
7.	W. Ranier, 'Nano Electronics and Information Technology', John Wiley & Sons, 2012.

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Course Content and Lecture Schedule

S. No	Topic	No. of Hours
1	**INTRODUCTION TO NANOELECTRONICS**	
1.1	Microelectronics towards biomolecule electronics	1
1.2	Particles and waves- Wave particle duality	1
1.3	Wave mechanics- Schrodinger wave equation	1
1.4	Wave mechanics of particles: Atoms and atomic orbitals	1
1.5	Materials for nanoelectronics- Semiconductors	1
1.6	Crystal lattices: Bonding in crystals- Electron energy bands	1
1.7	Semiconductor heterostructures- Lattice-matched and pseudomorphichetero structures	1
1.8	Inorganic-organic heterostructures	1
1.9	Carbon nanomaterials: nanotubes and fullerenes	1
2	**FABRICATION AND MEASUREMENT TECHNIQUES**	
2.1	Growth- fabrication- and measurement techniques for nanostructures	1
2.2	Bulk crystal and heterostructure growth	1
2.3	Nanolithography- etching- and other means for fabrication of nanostructures and nanodevices	1
2.4	Techniques for characterization of nanostructures	1
2.5	Spontaneous formation and ordering of nanostructures	1
2.6	Clusters and nanocrystals	1
2.7	Methods of nanotube growth	1
2.8	Chemical and biological methods for nanoscale fabrication	1
2.9	Fabrication of nano-electromechanical systems	1
3	**PROPERTIES**	
3.1	Dielectrics-Ferroelectrics, Electronic Properties and Quantum Effects	1
3.2	Magneto electronics – Magnetism and Magneto transport in Layered Structures	1
3.3	Organic Molecules	1
3.4	Electronic Structures	1
3.5	Properties- and Reactions-Neurons	1
3.6	The Molecular Basis of their Electrical Excitability	1
3.7	Circuit and System Design	1
3.8	Analysis by Diffraction and Fluorescence Methods	1
3.9	Scanning Probe Techniques	1
4	**NANO STRUCTURE DEVICES**	
4.1	Electron transport in semiconductors and nanostructures, Time and length scales of the electrons in solids	1
4.2	Statistics of the electrons in solids and nanostructures, Density of states of electrons in nanostructures	1
4.3	Electron transport in nanostructures	1
4.4	Electrons in traditional low-dimensional structures	1
4.5	Electrons in quantum wells, Electrons in quantum wires and Electrons in quantum dots	1
4.6	Nanostructure devices- Resonant-tunneling diodes	1

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4.7	Field-effect transistors, Single-electron transfer devices	1
4.8	Potential-effect transistors, Light-emitting diodes and lasers	1
4.9	Nano-electromechanical system devices- Quantum-dot cellular automata.	1
5	**LOGIC DEVICES AND APPLICATIONS**	
5.1	Logic Devices-Silicon MOSFETs	2
5.2	Ferroelectric Field Effect Transistors	1
5.3	Quantum Transport Devices Based on Resonant Tunneling	1
5.4	Single-Electron Devices for Logic Applications	1
5.5	Superconductor Digital Electronics	1
5.6	Quantum Computing Using Superconductors	1
5.7	Carbon Nanotubes for Data Processing	1
5.8	Molecular Electronics	1
	Total	45

Course Designers

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60 PVL E12	LINEAR ALGEBRA

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To understand the fundamental concepts of various vector spaces.
- To get the knowledge in linear transformations.
- To develop and analyze the canonical forms and Jordan canonical forms.
- To learn and implement procedure for inner product spaces.
- To solve the problems of linear algebra applications.

Prerequisite

Basic Linear Algebra

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the concepts of linear equations and vector spaces.	Remember, Understand, Apply
CO2	Apply principles of matrix algebra to linear transformations.	Remember, Understand, Apply
CO3	Compute the various canonical forms and structures to solve the problems.	Remember, Understand, Apply
CO4	Evaluate the inner product spaces and QR-factorization problems.	Remember, Apply, Evaluate
CO5	Acquire knowledge in the linear algebra applications.	Remember, Understand, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	
CO2	3	3	3	3	2	
CO3	3	3	3	2	2	
CO4	3	3	3	2	2	
CO5	3	3	2	2	2	

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	10	10	10
Understand (Un)	10	10	30
Apply (Ap)	40	30	50
Analyze (An)	0	0	0
Evaluate (Ev)	0	10	10
Create (Cr)	0	0	0
Total	60	60	100

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60 PVL E12- LINEAR ALGEBRA								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Linear Equations and Vector Spaces Linear equations: Fields- system of linear equations- and its solution sets - elementary row operations and echelon forms- matrix operations- invertible matrices- LU-factorization Vector Spaces: Vector spaces- subspaces- bases and dimension- coordinates- summary of row-equivalence-computations concerning subspaces.	[9]
Linear Transformations Linear Transformations: Linear transformations- algebra of linear transformations- isomorphism- representation of transformations by matrices- linear functionals- transpose of a linear transformation.	[9]
Canonical Forms Canonical Forms: Characteristic values- annihilating polynomials- invariant subspaces- direct-sum decompositions- invariant direct sums- primary decomposition theorem- cyclic bases- Jordan canonical form. Iterative estimates of characteristic values.	[9]
Inner Product Spaces Inner Product Spaces: Inner products- inner product spaces- orthogonal sets and projections- Gram-Schmidt process- QR-factorization- least-squares problems- unitary operators	[9]
Symmetric Matrices and Applications of Linear Algebra Symmetric Matrices and Quadratic Forms: Digitalization- quadratic forms- constrained optimization - singular value decomposition. Applications of Linear Algebra in DSP- Image Processing- Digital Communication.	[9]
Total Hours	**45**

Textbook(s):

1.	Gilbert Strang , 'Linear Algebra and its Applications', 4th Edition, Thomson, Brooks/Cole, 2013.
2.	David C. Lay, ,Steven R. LayJudith McDonald , 'Linear Algebra and its Applications', Pearson ,Education2016.

Reference(s):

1.	Bernard Kolman and David R. Hill, 'Introductory Linear Algebra: An Applied First Course', 9th Edition CRC press, 2014.
2.	T. Banchoff and J. Wermer, 'Linear Algebra through Geometry', Springer, 2012.
3.	S. Kumaresan, 'Linear Algebra: A geometric approach', Prentice Hall of India Private Ltd., 2013.
4.	Ganesh A, 'Linear Algebra and Its Applications',CBS Publishers & Distributors,2019

Course Contents and Lecture Schedule

S.No.	Topic	No.of Hours
1	**Linear Equations and Vector Spaces**	
1.1	Linear Equations: Fields	1
1.2	System of Linear Equations and its solutions	2
1.3	Elementary row operations and Echelon forms	1
1.4	Matrix operations, Invertible matrices	1
1.5	LU- factorization vector spaces, Vector spaces, subspaces	2
1.6	Bases and dimension coordinates, Summary of row equivalence	1
1.7	Computations Concerning subspaces	1

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2	**Linear Transformations**	
2.1	Linear transformations	2
2.2	Algebra of linear transformations	1
2.3	Isomorphism	1
2.4	Representation of transformations by matrices	1
2.5	Linear functionals	2
2.6	Transpose of a linear transformation	2
3	**Canonical Forms**	
3.1	Characteristic values	1
3.2	Annihilating polynomials	1
3.3	Invariant subspaces, Direct sum decompositions	2
3.4	Invariant direct sums	1
3.5	Primary decomposition theorem, Cyclic bases	2
3.6	Jordan canonical form	1
3.7	Iterative estimates of characteristic values	1
4	**Inner Product Spaces**	
4.1	Inner products	1
4.2	Inner product spaces	1
4.3	Orthogonal sets and projections	2
4.4	Gram- schmidt process	1
4.5	QR factorization	2
4.6	Least squares problems	1
4.7	Unitary operators	1
5	**Symmetric Matrices and Applications of Linear Algebra**	
5.1	Digitalization	1
5.2	Quadratic forms	2
5.3	Constrained optimization	1
5.4	Singular value decomposition	2
5.5	Applications of Linear algebra in DSP	1
5.6	Image processing,	1
5.7	Digital communication	1
	Total	45

Course Designers

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60 PVL E13	DIGITAL IMAGE PROCESSING	Category	L	T	P	Credit

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		PE	3	0	0	3

Objective

- To learn the image fundamentals and mathematical transform
- To analyse Image enhancement and restoration of image
- To analyse Image Segmentation And Recognition
- To Learn about color image processing and image compression
- To learn the image processing algorithms for image enhancement, restoration, and segmentation.

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe digital image fundamentals and different transforms.	Remember, Understand
CO2	Discuss the basics of Image enhancement and restoration techniques of images.	Apply
CO3	Explain the techniques of image segmentation and recognition.	Remember, Understand Apply, Analyse
CO4	Discuss about color image processing and image compression.	Apply, Analyse
CO5	Implement the image processing algorithms for image enhancement, restoration, and segmentation.	Apply, Analyse

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	3	3
CO2	3	3	3	2	3	3
CO3	3	3	3	2	3	3
CO4	3	3	3	2	3	3
CO5	3	3	3	2	3	3

1- low, 2- medium, 3- high

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	10	10	30
Understand(Un)	20	20	30
Apply (Ap)	30	30	30
Analyze (An)	0	0	10
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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60 PVL E13- DIGITAL IMAGE PROCESSING								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Digital Image Fundamentals and Transforms Elements of visual perception – Image sampling and quantization Basic relationship between pixels – Basic geometric transformations-Introduction to Fourier Transform and DFT – Properties of 2D Fourier Transform – FFT – Separable Image Transforms -Walsh – Hadamard – Discrete Cosine Transform – Haar - Slant – Karhunen Loeve transforms.	[9]
Image Enhancement and Restoration Basic gray level transformations – Histogram equalization – Histogram matching -spatial filtering – smoothing spatial filters – sharpening spatial filters- model of the image degradation / Restoration process- mean filters – order – statistics filters- Adaptive filters – Inverse filtering – minimum mean square error filtering – constrained least squares filtering – Geometric mean filter – geometric transformation.	[9]
Image Segmentation and Recognition Detection of Discontinuities – Edge linking and boundary detection – Region based segmentation – morphological operators: Dilation – erosion - opening and closing - Image recognition patterns and pattern classes. Recognition based on decision – theoretic methods.	[9]
Image Compression& Color Image Processing Need for data compression, Huffman, Run Length Encoding, Vector Quantization, Transform coding, JPEG standard, MPEG. Color Fundamentals – Color Models –Basics of Full-Color Image- Pseudo color Image Processing Processing-Color Transformations – Smoothing and Sharpening – Image Segmentation Based on Color	[9]
Simulation Implementation of Image processing algorithms - Image Enhancement - Restoration- Segmentation- Coding techniques- Applications.	[9]
	Total hours: 45

Text book(s):	
1.	Rafael C Gonzalez, Richard E. Woods, 'Digital Image Processing', Pearson Education, 4th Edition, 2018.
2.	A.K. Jain, 'Fundamentals of Digital Image Processing', New Edition, Prentice Hall of India, 2016.
Reference(s):	
1.	Yao Wang, JoernOstermann, and Ya-Qin Zhang ,' Video Processing and Communications', Prentice Hall, 2016.
2.	William K. Pratt, 'Digital Image Processing', John Wiley, New York, 2016
3.	Rafael C. Gonzalez Richard E. Woods, Steven Eddins, 'Digital Image Processing using MATLAB', Tata Mcgraw Hill, 2016.
4.	J.W. Woods, 'Multidimensional Signal, Image, Video Processing and Coding', 2nd Edition, Academic Press, 2016.

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S.No	Topic	No.of Hours
1	**Digital Image Fundamentals and Transforms**	
1.1	Elements of visual perception	1
1.2	Image sampling and quantization Basic relationship between pixels	1
1.3	Basic geometric transformations	1
1.4	Introduction to Fourier Transform and DFT	1
1.5	Properties of 2D Fourier Transform	1
1.6	FFT	1
1.7	Separable Image Transforms, Walsh, Hadamard	1
1.8	Discrete Cosine Transform	1
1.9	Haar – Slant, Karhunen Loeve transforms.	1
2	**Image Enhancement and Restoration**	1
2.1	Basic gray level transformations	1
2.2	Histogram equalization , Histogram matching	1
2.3	spatial filtering ,smoothing spatial filters	1
2.4	sharpening spatial filters- model of the image degradation / Restoration process	1
2.5	mean filters – order – statistics filters- Adaptive filters	1
2.6	Inverse filtering – minimum mean square error filtering	1
2.7	constrained least squares filtering	1
2.8	Geometric mean filter	1
2.9	geometric transformations	1
3	**Image Segmentation and Recognition**	1
3.1	Detection of Discontinuities	1
3.2	Edge linking and boundary detection	1
3.3	Region based segmentation	1
3.4	morphological operators: Dilation – erosion	2
3.5	opening and closing	1
3.6	Image recognition patterns and pattern classes	1
3.7	Recognition based on decision	1
3.8	theoretic methods	1
4	**Image Compression& Color Image Processing**	1
4.1	Need for data compression, Huffman	1
4.2	Run Length Encoding, Vector Quantization	1
4.3	Transform coding, JPEG standard, MPEG	1
4.4	Color Fundamentals – Color Models	1
4.5	Basics of Full-Color Image	1
4.6	Processing-Color Transformations	2
4.7	Smoothing and Sharpening	1
4.8	Image Segmentation Based on Color	1
5	**Simulation**	1
5.1	Implementation of Image processing algorithms	2

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5.2	Image Enhancement	2
5.3	Restoration	2
5.4	Segmentation	2
5.5	Coding techniques	2
5.6	Applications	1
Total		**45**

Course Designers

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60 PVL E14	IP BASED VLSI DESIGN

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To learn about IC manufacturing and fabrication.
- To analyse the combinational, sequential and subsystem design.
- To analyse the subsystem design.
- To learn about different floor planning techniques and architecture design.
- To introduce IP design security

Prerequisite

Digital CMOS VLSI Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the IC manufacturing with various fabrication process and Layout design techniques	Remember, Understand
CO2	Analyze the combinational logic networks and its functions	Apply
CO3	Design the sequential circuits and analyse the subsystem design performance	Understand, Apply
CO4	Describe the various floor planning techniques and architecture in VLSI.	Remember, Understand
CO5	Explain an IP based Protection of data and Privacy security.	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			3
CO2	3		3	3		3
CO3	3		3	3		3
CO4	3	3	3	3		3
CO5	3	3	3		3	3
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember (Re)	10	10	10
Understand (Un)	25	25	40
Apply (Ap)	25	15	40
Analyse (An)	0	10	10
Evaluate (Ev)	0	0	0
Create (Cr)	0	0	0
Total	60	60	100

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60 PVL E14- IP BASED VLSI DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

VLSI and Its Fabrication Introduction -IC manufacturing - CMOS technology - IC design techniques - IP based design - Fabrication process-Transistors - Wires and Vias - Fabrication Theory reliability - Layout Design and tools.	[9]
Combinational Logic Networks Logic Gates: Combinational Logic Functions - Static Complementary Gates - Switch Logic - Alternate Gate circuits - Low power gates – Delay – Yield - Gates as IP - Combinational Logic Networks-Standard Cell based Layout- Combinational network delay- Logic and Interconnect design- Power optimization- Switch logic network- logic testing.	[9]
Subsystem Design Sequential Machine -Latch and Flip flop - System design and Clocking - Performance analysis - power optimization - Design validation and testing - Subsystem Design-Combinational Shifter- Arithmetic Circuits- High Density memory - Image Sensors – FPGA – PLA - Buses and NoC - Data paths - Subsystems as IP.	[9]
Floor Planning and Architecture Design Floor planning -Floor planning methods - Global Interconnect - Floor plan design - Off -chip Connections Architecture Design - HDL - Register -Transfer Design - Pipelining - High Level Synthesis - Architecture for Low power - GALS systems - Architecture Testing - IP Components - Design Methodologies - Multiprocessor System - on-chip Design	[9]
Design Security IP in reuse based design - Constrained based IP protection - Protection of data and Privacy constrained based watermarking for VLSI IP based protection	[9]
Total hours	**45**

Text book(s):

1. Wayne wolf, 'Modern VLSI Design: IP-based Design', 4th Edition, Prentice Hall of India Private Ltd., 2013.
2. Qu gang, MiodragPotkonjak, 'Intellectual Property Protection in VLSI Designs: Theory and Practice', Springer, 2013.

Reference(s):

1. Marilyn Wolf, 'Modern VIsi Design Ip-Based Design', 4th Edition Prentice Hall of India Private Ltd., 2013.
2. Swarup Bhunia, SandipRay, Susmita Sur-Kolay, 'Fundamentals of IP and SoC Security: Design,Verification and .Debug', Springer,2017
3. Prabhat Mishra, ,Swarup Bhunia' ,Mark TehranipoorHardware IP Security and Trust', Springer, 2017.
4. Charlotte Stedman, 'Modern VLSI Design', Larsen & Keller Education, 2019

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**VLSI and Its Fabrication**	
1.1	Introduction -IC manufacturing	1
1.2	CMOS technology	1
1.3	IC design techniques	1
1.4	IP based design	1
1.5	Fabrication process	1
1.6	Transistors	1
1.7	Wires and Vias	1
1.8	Fabrication Theory reliability	1

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1.9	Layout Design and tools	1
2	**Combinational Logic Networks**	
2.1	Logic Gates: Combinational Logic Functions	1
2.2	Static Complementary Gates	1
2.3	Switch Logic - Alternate Gate circuits	1
2.4	Low power gates	1
2.5	Delay, Yield, Gates as IP	1
2.6	Combinational Logic Networks	1
2.7	Standard Cell based Layout	1
2.8	Combinational network delay, Logic and Interconnect design	1
2.9	Power optimization, Switch logic network, logic testing.	1
3	**Subsystem Design**	
3.1	Sequential Machine -Latch and Flip flop	1
3.2	System design and Clocking	1
3.3	Performance analysis	1
3.4	power optimization, Design validation and testing	1
3.5	Subsystem Design, Combinational Shifter	1
3.6	Arithmetic Circuits	1
3.7	High Density memory, Image Sensors	1
3.8	FPGA, PLA	1
3.9	Buses and NoC, Data paths, Subsystems as IP	1
4	**Floor Planning and Architecture Design**	
4.1	Floor planning, Floor planning methods	1
4.2	Global Interconnect, Floor plan design	1
4.3	Off -chip Connections Architecture Design	1
4.4	HDL, Register, Transfer Design	1
4.5	Pipelining, High Level Synthesis	1
4.6	Architecture for Low power, GALS systems	1
4.7	Architecture Testing, IP Components	1
4.8	Design Methodologies,	1
4.9	Multiprocessor System, on-chip Design	1
5	**Design Security**	
5.1	IP in reuse-based design	2
5.2	Constrained based IP protection	2
5.3	Protection of data and Privacy.	2
5.4	constrained based watermarking for VLSI IP based protection	3
	Total	45

Course Designers

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60 PVL E15	GENETIC ALGORITHM FOR VLSI DESIGN

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To introduce overview of Genetic algorithms.
- To design and analyse GA for VLSI design
- To study the advanced GAs.
- To introduce the GA for VLSI testing
- To study the applications of GA in VLSI

Prerequisite

Digital CMOS VLSI Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the fundamentals genetic algorithms	Remember, Understand
CO2	Design and analyze the Genetic Algorithms for VLSI design	Analyze
CO3	Design and analyze the Advanced Genetic Algorithms for VLSI design	Analyze
CO4	Design and analyze the Genetic Algorithm for VLSI testing	Analyze
CO5	Analyse the applications of GA in VLSI deign	Analyze

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			3
CO2	3		3	3		3
CO3	3		3	3		3
CO4	3	3	3	3		3
CO5	3	3	3		3	3
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	0	0	0
Understand(Un)	10	10	20
Apply (Ap)	25	25	30
Analyze (An)	25	25	50
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E15 - GENETIC ALGORITHM FOR VLSI DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

OVERVIEW OF GENETIC ALGORITHMS Introduction to GA Technology - Simple GA algorithm -Steady State Algorithm - Selection - Crossover - Mutation - Fitness Scaling – Inversion	[9]
GENETIC ALGORITHM FOR VLSI DESIGN GA for VLSI Design, Layout and Test automation - Partitioning - Automatic Placement - Automatic Routing - Technology mapping for FPGAs - Automatic test generation - Genetic Multiway Partitioning	[9]
ADVANCED GENETIC ALGORITHMS Hybrid genetic - Genetic encoding - Local improvement - WDFR - Comparison of CAs - Standard cell placement - GASP algorithm - Unified algorithm.	[9]
GENETIC ALGORITHM FOR VLSI TESTING Macro Cell Global routing - FPGA technology mapping - Circuit segmentation - Test generation in a GA frame work - Test generation procedures.	[9]
APPLICATIONS Power estimation - Application of GA - Standard cell placement - GA for ATG - Problem Encoding - Fitness function - GA vs Conventional Algorithm.	[9]
Total hours	**45**

Text book(s):	
1.	Pinaki Mazumder, E.MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1999
2.	Pinaki Mazumder, E.MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1999
Reference(s):	
1.	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 2001.
2.	M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley, 1997
3.	John R.Koza, Forrest H.Bennett, David Andre, Morgan Kufmann, "Genetic Programming: Automatic Discovery of Reusable Programs", MIT Press, 1999.

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**OVERVIEW OF GENETIC ALGORITHMS**	
1.1	Introduction to GA Technology	2
1.2	Simple GA algorithm	1
1.3	Steady State Algorithm	1
1.4	Selection	1
1.5	Crossover	1
1.6	Mutation	1
1.7	Fitness Scaling	1
1.8	Inversion	1
2	**GENETIC ALGORITHM FOR VLSI DESIGN**	
2.1	GA for VLSI Design	1
2.2	Layout and Test automation	2
2.3	Partitioning - Automatic Placement	2

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2.4	Automatic Routing	1
2.5	Technology mapping for FPGAs	1
2.6	Automatic test generation	1
2.7	Genetic Multiway Partitioning	1
3	**ADVANCED GENETIC ALGORITHMS**	
3.1	Hybrid genetic	1
3.2	Genetic encoding	1
3.3	Local improvement	1
3.4	WDFR	1
3.5	Comparison of CAs	1
3.6	Standard cell placement	1
3.7	GASP algorithm	2
3.8	Unified algorithm	1
4	**GENETIC ALGORITHM FOR VLSI TESTING**	
4.1	Macro Cell Global routing	1
4.2	FPGA technology mapping	2
4.3	Circuit segmentation	2
4.4	Test generation in a GA frame work	2
4.5	Test generation procedures	2
5	**APPLICATIONS**	
5.1	Power estimation	1
5.2	Application of GA	1
5.3	Standard cell placement	1
5.4	GA for ATG	2
5.5	Problem Encoding	1
5.6	Fitness function	1
5.7	GA vs Conventional Algorithm	2
	Total	45

Course Designers

1. Mr D Mugilan – mugilan@ksrct.ac.in

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60 PVL E16	BIO SIGNAL PROCESSING

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To Know the basic concept of signals and systems and their spectrums
- Analyze the Spectral estimation
- Apply the concept of adaptive filtering and their wavelets in biosignals
- Explain biosignal classification
- Carry out multivariate component analysis

Prerequisite

Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	know the characteristics basic signals, system and spectrums	Remember, Understand
CO2	Analyze the Bio signals in time domain and spectral estimation	Apply, Analyze
CO3	Analyze the Adaptive filtering and wavelet detection in ECG	Apply, Analyze
CO4	Explain bio signal classification	Remember, Understand
CO5	analyze the multivariate components in time frequency domains	Remember, Understand, Analyze

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3		
CO2	3	3	3	3		
CO3	3	3	3	3	3	
CO4	3	3	3	3	3	
CO5	3	3	3	3		

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	20	20	20
Understand(Un)	20	20	40
Apply (Ap)	10	10	20
Analyze (An)	10	10	20
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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60 PVL E16- BIO SIGNAL PROCESSING								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
II	3	0	0	45	3	40	60	100

SIGNAL, SYSTEM AND SPECTRUM Characteristics of some dynamic biomedical signals, Noises-random, structured and physiological noises, Filters-IIR and FIR filters, Spectrum- power spectral density function, cross-spectral density and coherence function, cepstrum and homomorphic filtering, Estimation of mean of finite time signals.	[9]
TIME SERIES ANALYSIS AND SPECTRAL ESTIMATION Time series analysis- linear prediction models, process order estimation, non-stationary process, fixed segmentation, adaptive segmentation, application in EEG, PCG and HRV signals, model based ECG simulator, spectral estimation-Blackman Tukey method, periodogram and model based estimation, Application in heart rate variability, PCG signals.	[9]
ADAPTIVE FILTERING AND WAVELET DETECTION Filtering-LMS adaptive filter, adaptive noise cancelling in ECG, improved adaptive filtering in FECG, EEG and other applications in Bio signals, Wavelet detection in ECG- Structural features, matched filtering, adaptive wavelet detection, detection of overlapping wavelets.	[9]
BIOSIGNAL CLASSIFICATION AND RECOGNITION Signal classification and recognition- statistical signal classification, linear discriminant function, direct feature selection and ordering, back propagation neural network based classification, Application in Normal versus Ectopic ECG beats and other biomedical applications	[9]
TIME FREQUENCY AND MULTIVARIATE ANALYSIS Time frequency representation, spectrogram, Time-scale representation, scalogram, wavelet analysis-Data reduction techniques, ECG data compression, ECG characterization, Feature extraction- Wavelet packets, Multivariate component analysis –PCA, ICA.	[9]
	Total hours: 45

Reference(s):

1.	Arnon Cohen, Bio-medical Signal Processing Vol I and Vol II, CRC Press Inc., Boca Rato, Florida 1999.
2.	Emmanuvel C.ifeachor, Barrie W.Jervis, Second edition “Digital Signal Processing-A Practical approach” , Pearson education Ltd., 2002
3.	P.Ramesh Babu, “Digital Signal Processing”, Sixth Edition, Scitech publications, Chennai, 2014.
4.	Raguveer M.Rao and AjithS.Bopardikar, Wavelets Transform-Introduction to theory and its applications, Pearson Education, India 2000.
5	Rangaraj M.Rangayyan, 2nd edition, “Biomedical Signal Analysis-A case study approach”, Wiley, IEEE Press, 2015.

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours

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1	**SIGNAL, SYSTEM AND SPECTRUM**	
1.1	Characteristics of some dynamic biomedical signals	1
1.2	Noises-random, structured and physiological noises	1
1.3	FIR Filters	1
1.4	IIR filters	1
1.5	Power Spectral Density function	1
1.6	Cross spectral density function	1
1.7	Coherence function	1
1.8	Cepstrum and homomorphic filtering	1
1.9	Estimation of mean of finite time signals	1
2	**TIME SERIES ANALYSIS AND SPECTRAL ESTIMATION**	
2.1	Time series analysis, linear prediction models	1
2.2	Process order estimation	1
2.3	Non stationary process	1
2.4	Fixed segmentation and adaptive segmentation	1
2.5	Application in EEG,PCG and HRV signals	1
2.6	Model Based ECG Simulator	1
2.7	Spectral Estimation, Blackman Tuckey method	1
2.8	Periodogram and model based estimation	1
2.9	Application in heart rate variability, PCG Signals	1
3	**ADAPTIVE FILTERING AND WAVELET DETECTION**	
3.1	Filtering, LMS Adaptive filter	1
3.2	Adaptive noise cancelling in ECG	1
3.3	Improved adaptive filtering in FECG	1
3.4	EEG and other applications in Bio Signals	1
3.5	Wavelet Detection in ECG	1
3.6	Structural features	1
3.7	Matched filtering	1
3.8	Adaptive Wavelet Detection	1
3.9	Detection of overlapping wavelets	1
4	**BIOSIGNAL CLASSIFICATION AND RECOGNITION**	
4.1	Signal Classification and recognition	1
4.2	Statistical Signal Classification	1
4.3	Linear discriminant function	1
4.4	Direct feature selection and ordering	2
4.5	Back Propagation neural network based classification	2
4.6	Application in Normal versus Ectopic ECG beats	1
4.7	Other medical applications	1
5	**TIME FREQUENCY AND MULTIVARIATE ANALYSIS**	
5.1	Time frequency representation, Spectrogram	1
5.2	Time Scale Representation,	1
5.3	Scalogram	1
5.4	Wavelet Analysis, data reduction techniques	1

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5.5	ECG data Compression	1
5.6	ECG Data Characterization	1
5.7	feature extraction	1
5.8	Wavelet Packets	1
5.9	Multivariate Component Analysis-PCA, ICA	1
	Total	45

Course Designers

1. Mr.P.Balamurugan –pbalamurugan@ksrct.ac.in

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60 PVL E21	VLSI FOR WIRELESS COMMUNICATION

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To learn the design concepts of low noise amplifiers.
- To learn the various types of mixers designed for wireless communication.
- To learn and design PLL and VCO.
- To know the concepts of data converters in communication
- To learn the concepts of CDMA in wireless communication.

Prerequisite

Fundamentals of VLSI and Wireless Communication

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the concept of MOSFET and BJT Amplifier design.	Remember, Understand Analyze
CO2	Describe the concept of Mixer	Remember, Understand Apply
CO3	Describe the concept of frequency Synthesizers	Remember, Apply
CO4	Know the basic concept of data converters in communications.	Remember, Understand, Analyze
CO5	Describe the VLSI Implementation concept for wireless System.	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	
CO2	3	3	3	3	
CO3	3	3	3	3	
CO4	3	2	3	3	3
CO5	3	2	3	3	3
1- low, 2- medium, 3- high					

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	20	20	20
Understand(Un)	10	10	20
Apply (Ap)	20	30	50
Analyze (An)	10	0	10
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E21- VLSI FOR WIRELESS COMMUNICATION								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Note: Hours notified against each unit in the syllabus are only indicative but are not decisive. Faculty may decide the number of hours for each unit depending upon the concepts and depth. Questions need not be asked based on the number of hours notified against each unit in the syllabus.

Components and Devices Integrated inductors- resistors- MOSFET and BJT Amplifier Design: Low Noise Amplifier Design - WidebandLNA - Design Narrowband LNA - Impedance Matching-Matching of Imaginary and real Part-Interpretation of Power Matching - Automatic Gain Control Amplifiers – Power Amplifiers.	[9]
Mixers Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise – A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer - Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.	[9]
Frequency Synthesizers Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).	[9]
Sub Systems Data converters in communications - adaptive Filters - equalizers and transceivers	[9]
Implementations VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System	[9]
	Total hours: 45

Text book(s):	
1.	B.Razavi , 'RF Microelectronics' , 2nd Edition Prentice Hall of India Private Ltd.,2013.
2.	Bosco H. Leung, 'VLSI for Wireless Communication', 2nd Edition, Springer US, 2014.
Reference(s):	
1.	Lee,Thomas H.Lee, 'The Design of CMOS Radio Frequency Integrated Circuits', 2nd Edition,Cambridge University Press, 2013.
2.	Emad N Farag, Mohamed I. Elmasry, 'Mixed Signal VLSI Wireless Design: Circuits and Systems', Springer US, 2013.
3.	BehzadRazavi, 'Design of Analog CMOS Integrated Circuits', Tata McGraw Hill, 2012.
4.	J. Crols and M. Steyaert, 'CMOS Wireless Transceiver Design', Springer, 2013.

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**COMPONENTS AND DEVICES**	
1.1	Integrated inductors- resistors	2
1.2	MOSFET and BJT Amplifier Design: Low Noise Amplifier Design	2
1.3	WidebandLNA - Design Narrowband LNA	2
1.4	Impedance Matching-Matching of Imaginary and real Part-Interpretation of Power	2

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	Matching	
1.5	Automatic Gain Control Amplifiers – Power Amplifiers	1
2	**MIXERS**	
2.1	Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion	1
2.2	– Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise – A Complete Active Mixer	2
2.3	Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer	2
2.4	Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer	1
2.5	Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer	1
2.6	Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer	1
2.7	Extrinsic Noise in Single Ended Sampling Mixer.	1
3	**FREQUENCY SYNTHESIZERS**	
3.1	Phase Locked Loops - Voltage Controlled Oscillators	1
3.2	Phase Detector – Analog Phase Detectors	2
3.3	Digital Phase Detectors - Frequency Dividers	2
3.4	LC Oscillators - Ring Oscillators	1
3.5	Phase Noise	2
3.6	A Complete Synthesizer Design Example (DECT Application).	1
4	**SUB SYSTEMS**	
4.1	Introduction to subsystems	1
4.2	Data converters in communications (Analog)	2
4.3	Data converters in communications (Digital)	2
4.4	Adaptive Filters	2
4.5	Equalizers	1
4.6	Transceivers	1
5	**IMPLEMENTATIONS**	
5.1	Introduction	2
5.2	VLSI architecture for Multitier Wireless System	3
5.3	Introduction to CDMA	2
5.4	Hardware Design Issues for a Next generation CDMA System	2
	Total	45

Course Designers

1. Mr.R.Satheeshkumar – satheeshkumar@ksrct.ac.in

60 PVL E22	SYSTEM ON CHIP	Category	L	T	P	Credit

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		PE	3	0	0	3

Objective

- To introduce architecture and design concepts underlying system on chips.
- To explain the knowledge of designing SoCs.
- To learn impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications.
- To learn the modeling, synthesis and physical design.
- To learn the various FPGA base Embedded Processor

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain all important components of a System-on-Chip and an embedded system,	Remember, Understand
CO2	Learn the digital hardware and Embedded software	Remember, Understand
CO3	Outline the major design flows for digital hardware and embedded software	Apply
CO4	Describe the major architectures and trade-offs concerning performance, cost and power	Remember, Understand
CO5	Outline the Consumption of single chip and embedded systems	Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2	PEO3
CO1	3	3					3	3	
CO2	3	3		3		3	3	3	
CO3	3	3					3	2	
CO4	3	3		3		3	3	3	
CO5	3	3		3		3	3	3	
1- low, 2- medium, 3- high									

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	20	20	30
Understand(Un)	30	20	40
Apply (Ap)	10	20	30
Analyze (An)	0	0	0
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

SYSTEM ARCHITECTURE: OVERVIEW Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.	[9]
PROCESSOR SELECTION FOR SOC Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.	[9]
MEMORY DESIGN SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D caches – multilevel caches – SoC memory systems – board-based memory systems – simple processor/ Memory interaction.	[9]
INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION Bus architectures – SoC standard buses – AMBA, Core Connect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.	[9]
FPGA BASED EMBEDDED PROCESSOR Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.	[9]
	Total hours: 45

Text book(s):	
1.	Michael J.Flynn and Wayne Luk, "Computer system design system on Chip", Wiley India Pvt. Ltd.
2.	Steve Furber, " ARM system on Chip Architecture ", 2nd Edition, 2000, Addison Wesley Professional.
Reference(s):	
1.	Veena S.Chakravarthi, 'A Practical Approach to VLSI System On Chip Design', Springer, 2020.
2.	Rainer Leupers, Olivier Temam, 'Processor and System on Chip Simulation', Springer, 2010.

Course Contents and Lecture Schedule

S. No	Topic	No. of Hours
1	**SYSTEM ARCHITECTURE: OVERVIEW**	

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1.1	Components of the system	1
1.2	Processor architectures	1
1.3	Memory and addressing	1
1.4	system level interconnection	1
1.5	SoC design requirements and specifications	1
1.6	design integration and design complexity	1
1.7	cycle time, die area and cost, ideal and practical scaling	1
1.8	Area-time-power tradeoff in processor design	1
1.9	Configurability	1
2	**PROCESSOR SELECTION FOR SOC**	
2.1	soft processors, processor core selection - Overview	1
2.2	Basic concepts – instruction set, branches, interrupts and exceptions	1
2.3	Basic elements in instruction handling	1
2.4	Minimizing pipeline delays	1
2.5	Reducing the cost of branches	1
2.6	Robust processors	1
2.7	Vector processors	1
2.8	VLIW processors	1
2.9	Superscalar processors	1
3	**MEMORY DESIGN**	
3.1	SoC external memory, SoC internal memory	1
3.2	Scratch pads and cache memory	1
3.3	cache organization and write policies	1
3.4	strategies for line replacement at miss time	1
3.5	split I- and D caches	1
3.6	multilevel caches	1
3.7	SoC memory systems	1
3.8	board based memory systems	1
3.9	simple processor/ Memory interaction	1
4	**INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION**	
4.1	Bus architectures - Introduction	1
4.2	SoC standard buses	1
4.3	AMBA, Core Connect	1
4.4	Processor customization approaches	1
4.5	Reconfigurable technologies	1
4.6	mapping designs onto reconfigurable devices	1
4.7	FPGA based design	1
4.8	Architecture of FPGA, FPGA interconnect technology	1
4.9	FPGA memory, Floor plan and routing	1
5	**FPGA BASED EMBEDDED PROCESSOR**	
5.1	Hardware software task partitioning	1
5.2	FPGA fabric Immersed Processors	1
5.3	Soft Processors and Hard Processors	1
5.4	Tool flow for Hardware/Software Co-design	1

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5.5	Interfacing Processor with memory and peripherals	1
5.6	Types of On-chip interfaces	1
5.7	Wishbone interface, Avalon Switch Matrix, OPB Bus Interface	1
5.8	Creating a Customized Microcontroller	1
5.9	FPGA-based Signal Interfacing and Conditioning	1
	Total	45

Course Designers

1. Mr.K.Rajasekar – rajasekar@ksrct.ac.in

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60 PVL E23	MACHINE LEARNING TECHNIQUES

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To introduce the basic concepts and techniques of machine learning
- To familiarize the theoretical and practical aspects of linear models
- To study various dimensionality reduction techniques and distance based models
- To learn the theoretical and practical aspects of probabilistic graphic models
- To expose the concepts of reinforcement learning and its applications.

Prerequisite

NIL

CourseOutcomes

On the successful completion of the course, students will be able to

CO1	Learn the mathematical foundations for machine learning.	Remember, Understand
CO2	Apply the appropriate machine learning techniques for classification and regression	Apply
CO3	Realize the concepts of clustering and dimensionality reduction techniques.	Apply,Analyse
CO4	Understand the learning algorithm for graphical model and ensemble methods	Apply, Analyse
CO5	Understand the basic concept of reinforcement leaning and its applications	Understand, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		2	
CO2	3		3	2	3	
CO3	3		3	2	3	
CO4	3		3	2	3	
CO5	3		3	2	3	
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	10	20	10
Understand(Un)	20	20	40
Apply (Ap)	30	20	50
Analyze (An)	0	0	0
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E23 - MACHINE LEARNING TECHNIQUES								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction Probability theory - model selection - Decision theory - Information theory - Entropy and mutual information. Types of machine learning - Supervised learning - Unsupervised learning - Reinforcement learning – Bias and variance – learning curve - Machine Learning applications	[9]
Linear Models Linear regression- Logistic regression- Perceptrons- Support Vector Machines - hard SVM, soft SVM - Classification and Regression Trees- Generalization and Overfitting – Regularization	[9]
Distance Based Models & Dimensionality Reduction Nearest neighbour models - K means - clustering around medoids - Hierarchical clustering - Decision tree - Univariate tree - Multivariate trees - Dimensionality reduction - Principle Component Analysis - Linear Discriminant Analysis	[9]
Graphical Model & Ensemble Methods: Undirected graphical models, HMM, Variable Elimination, Belief Propagation Ensemble methods - Bagging, Committee Machines and Stacking, Boosting - Adaboost, Gradient Boosting, Random Forest, Naive Bayes, Bayesian networks.	[9]
Reinforcement learning Elements of reinforcement learning - Model based learning - Temporal Difference learning – Generalization, Learning an action -utility function – Policy search – Applications in Health care	[9]
	Total hours: 45

Text book(s):	
1.	Peter Flach, 'Machine Learning: The art and science of algorithms that make sense of data', Cambridge University Press, 2012.
2.	Christopher M. Bishop, 'Pattern Recognition and Machine Learning', Springer, 2013.
Reference(s):	
1.	Tom M Mitchell, 'Machine Learning',1st Edition, McGraw Hill Education,2017
2.	K. P. Murphy, 'Machine Learning: A probabilistic perspective', MIT Press, 2012.
3.	Stephen Marshland, Machine Learning: An Algorithmic Perspective, 2nd edition,2014
4.	Ethem Alpaydin, 'Introduction to Machine Learning', MIT Press, Prentice Hall of India, 2010.

Course Contents and Lecture Schedule

S.No	Topic	No.of Hours
1	**Introduction**	
1.1	Probability theory	1
1.2	model selection	1
1.3	Decision theory	1
1.4	Information theory	1
1.5	Entropy and mutual information	2
1.6	Types of machine learning - Supervised learning - Unsupervised learning - Reinforcement learning	1
1.7	Bias and variance – learning curve	1
1.8	Machine Learning applications	1

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S.No	Topic	No.of Hours
2	**Linear Models**	
2.1	Linear regression	2
2.2	Logistic regression	1
2.3	Perceptrons	2
2.4	Support Vector Machines - hard SVM, soft SVM	1
2.5	Classification and Regression Trees-	1
2.6	Generalization and Overfitting	1
2.7	Regularization.	1
3	**Distance Based Models & Dimensionality Reduction**	
3.1	Nearest neighbour models- K means	2
3.2	clustering around medoids	1
3.3	Hierarchical clustering -	1
3.4	Decision tree	1
3.5	Univariate tree - Multivariate trees	1
3.6	Dimensionality reduction	1
3.7	Principle Component Analysis	1
3.8	Linear Discriminant Analysis.	1
4	**Graphical Model & Ensemble Methods:** .	
4.1	Undirected graphical models	1
4.2	HMM	1
4.3	Variable Elimination, Belief Propagation	1
4.4	Ensemble methods – Bagging	1
4.5	Committee Machines and Stacking	1
4.6	Boosting - Adaboost, Gradient Boosting	1
4.7	Random Forest	1
4.8	Naive Bayes, Bayesian networks	2
5	**Reinforcement learning**	
5.1	Elements of reinforcement learning	2
5.2	Model based learning	1
5.3	Temporal Difference learning	1
5.4	Generalization	1
5.5	Learning an action -utility function	1
5.6	Policy search	1
5.7	Applications in Health care.	8

Course Designers

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

60 PVL E24	FPGA BASED IMPLEMENTATION OF SIGNAL PROCESSING SYSTEMS

Category	L	T	P	Credit
PE	3	0	0	3

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Objective

- To learn the basics of FPGAs and DSP systems.
- To learn the different types of FPGA technologies.
- To understand the architectures and tools for FPGA based DSP systems.
- To know the concepts of IP cores and implementation for FPGA DSP systems.
- To learn low power FPGA Implementation

Prerequisite

Digital Logic Design and Digital Signal processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the fundamental of FPGAs and computer arithmetic unit of DSP systems	Remember, Understand
CO2	Analyze various FPGA technologies and implementation for DSP systems	Apply
CO3	Know the design requirements, concept and tools for FPGA based DSP architectures	Understand, Apply
CO4	Learn the concept of IP cores for FPGA complex DSP systems	Remember, Understand
CO5	Explain the power reduction techniques and architecture for low power FPGA implementation and application of FFT in VLSI	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3		
CO2	3	3	3	3		
CO3	3	3	3	3	3	
CO4	3	3	3	3	3	
CO5	3	3	3	3		
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	20	10	30
Understand(Un)	10	10	20
Apply (Ap)	30	30	30
Analyze (An)	0	10	20
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E24 - FPGA BASED IMPLEMENTATION OF SIGNAL PROCESSING SYSTEMS								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
II	3	0	0	45	3	40	60	100

Fundamentals of FPGAs and DSP Introduction to Field-programmable Gate Arrays, A Short History of the Microchip, Influence of Programmability, Challenges of FPGAs, DSP System Basics, DSP System Definitions, DSP Transforms, Filter Structures, Adaptive Filtering, Basics of Adaptive Filtering, Number Systems, Fixed-point and Floating-point, Arithmetic Operations, Fixed-point versus Floating-point.	[9]
FPGA technologies and implementation issues Xilinx FPGA Technologies, Altera FPGA Technologies, Various Forms of the LUT, Memory Availability Fixed Coefficient Design Techniques, Distributed Arithmetic, Reduced Coefficient Multiplier	[9]
Architectures and tools for FPGA based DSP systems The Evolution of FPGA System Design, Design Methodology Requirements for FPGA DSP, System Specification, IP Core Generation Tools for FPGA, System-level Design Tools for FPGA, DSP Algorithm Characteristics, DSP Algorithm Representations, Basics of Mapping DSP Systems onto FPGAs, Parallel Operation, Hardware Sharing, Application to FPGA.	[9]
Complex DSP systems Motivation for Design for Reuse, Intellectual Property (IP) Cores, Evolution of IP Cores, Parameterizable (Soft) IP Cores, IP Core Integration, IP Core Example, Current FPGA-based IP Cores, Dataflow Modeling and Rapid Implementation for FPGA DSP Systems, System-level Design and Exploration of Dedicated Hardware.	[9]
Low Power FPGA Implementation Sources of Power Consumption, Power Consumption Reduction Techniques, Voltage Scaling in FPGAs, Reduction in Switched Capacitance, Data Reordering, Fixed Coefficient Operation, Pipelining, Locality,Application to an FFT Implementation, Reconfigurable Systems, Memory Architectures, Support for Floating- point Arithmetic.	[9]
	Total hours: 45

Text book(s):	
1.	Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, 'FPGA-based Implementation of Signal Processing Systems',2nd Edition, John Wiley and Sons, 2017.
2.	Wayne Wolf, 'FPGA-Based System Design', Prentice Hall, New Delhi, 2012.
Reference(s):	
1.	Uwe Meyer Baese, 'Digital Signal Processing with Field Programmable Gate Arrays', 4th Edition, Springer, 2014.
2.	Neil H.E.Weste, Kamran Eshraghian, 'Principles of CMOS VLSI Design', 2nd Edition, Pearson, 1993.
3.	John G.Proakis, Dimitris Manolakis,'Digital Signal Processing: Principles, Algorithms and Applications', 4th Edition, Pearson Education, 2014.
4.	Sanjit K.Mitra, 'Digital Signal Processing: A Computer based approach', 4th Edition, McGraw-Hill, 2013.

Course Contents and Lecture Schedule

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S.No	Topic	No. of Hours
1	**Fundamentals of FPGAs and DSP**	
1.1	Introduction to Field-programmable Gate Arrays	1
1.2	A Short History of the Microchip, Influence of Programmability,	1
1.3	Challenges of FPGAs	1
1.4	DSP System Basics, DSP System Definitions	1
1.5	DSP Transforms,	1
1.6	Filter Structures,	1
1.7	Adaptive Filtering, Basics of Adaptive Filtering	1
1.8	Number Systems, Fixed-point and Floating-point	1
1.9	Arithmetic Operations, Fixed-point versus Floating-point	1
2	**FPGA technologies and implementation issues**	
2.1	Xilinx FPGA Technologies	2
2.2	Altera FPGA Technologies	2
2.3	Various Forms of the LUT	2
2.4	Memory Availability Fixed Coefficient Design Techniques	1
2.5	Distributed Arithmetic	1
2.6	Reduced Coefficient Multiplier	1
3	**Architectures and tools for FPGA based DSP systems**	
3.1	The Evolution of FPGA System Design	1
3.2	Design Methodology Requirements for FPGA DSP	1
3.3	System Specification, IP Core Generation Tools for FPGA	1
3.4	System-level Design Tools for FPGA	1
3.5	DSP Algorithm Characteristics	1
3.6	DSP Algorithm Representations	1
3.7	Basics of Mapping DSP Systems onto FPGAs	1
3.8	ParallelOperation	1
3.9	Hardware Sharing, Application to FPGA	1
4	**Complex DSP systems**	
4.1	Motivation for Design for Reuse	1
4.2	Intellectual Property (IP) Cores	1
4.3	Evolution of IP Cores, Para meterizable (Soft) IP Cores	1
4.4	Para meterizable (Soft) IP Cores	1
4.5	IP Core Integration, IP Core Example	1
4.6	Current FPGA-based IP Cores	1
4.7	Data flow Modeling and Rapid Implementation for FPGA DSP Systems	1
4.8	System-level Design	1
4.9	Exploration of Dedicated Hardware	1
5	**Low Power FPGA Implementation**	
5.1	Sources of Power Consumption	1
5.2	Power Consumption Reduction Techniques	1
5.3	Voltage Scaling in FPGAs	1
5.4	Reduction in Switched Capacitance	1

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S.No	Topic	No. of Hours
5.5	Data Reordering	1
5.6	Fixed Coefficient Operation	1
5.7	Pipelining, Locality,	1
5.8	Application to an FFT Implementation, Reconfigurable Systems	1
5.9	Reconfigurable Systems, Memory Architectures, Support for Floating- point Arithmetic.	1
	Total	45

Course Designers

1. Mr.P.Balamurugan – pbalamurugan@ksrct.ac.in

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60 PVL E25	NETWORK ON CHIP

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- Understand the concept of Network - on - Chip
- Learn router architecture designs
- Study routing algorithm
- Study fault tolerance Network - on – Chip
- Learn Three-Dimensional Network on chip architectures

Prerequisite

Interconnection Networks

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Compare different architecture design	Analyse
CO2	Discuss different routing algorithms	Remember, Understand
CO3	Explain three dimensional Networks on Chip architectures	Remember, Understand, Apply
CO4	Test and design fault tolerant NOC	Understand, Create
CO5	Design three dimensional architectures of NOC	Create

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3			3
CO2	3	3	3			3
CO3	3	3		3	3	3
CO4	3	3	3	3		3
CO5	3	3	3		3	3
1- low, 2- medium, 3- high						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	15	15	30
Understand(Un)	20	20	30
Apply (Ap)	25	25	30
Analyze (An)	0	0	10
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E25 - NETWORK ON CHIP								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

INTRODUCTION TO NOC Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality- of-Service Support	[9]
ARCHITECTURE DESIGN Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design	[9]
ROUTING ALGORITHM Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms.	[9]
TEST AND FAULT TOLERANCE OF NOC Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance for Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips	[9]
THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks- On-Chip	[9]
Total hours	**45**

Text book(s):	
1.	Chrysostomos Nicopoulos. Vijaykrishnan Narayanan • Chita R. Das. Network-on-Chip. Architectures. A . Holistic Design Exploration", Springer
2.	Fayez gebali, Haytham elmiligi, MohamedWatheq , E1-Kharashi "Networks-On-Chips Theory and Practice CRC Press
3.	Giovanni De Micheli, Luca Benini, Davide Bertozzi, Networks on Chips:Technology and Tools, Morgan Kaufmann, 2006.
Reference(s):	
1.	Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013
2.	Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-On-Chip" 2014
3.	Sudeep Pasricha, NikilDutt, On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann, 2010
4.	José Flich and Davide Bertozzi, Designing Network On-Chip Architectures in the Nanoscale Era, Chapman and Hall/CRC, 2011

Course Contents and Lecture Schedule

S.No	Topic	No.of Hours
1	**INTRODUCTION TO NOC**	
1.1	Introduction to NOC	1
1.2	OSI Layer Rules in NOC	1
1.3	Interconnection Networks in Network-On-Chip Network Topologies	2
1.4	Switching Techniques	1
1.5	Routing Strategies	2
1.6	Flow Control Protocol Quality- of-Service Support	2
2	**ARCHITECTURE DESIGN**	

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S.No	Topic	No.of Hours
2.1	Switching Techniques and Packet Format	2
2.2	Asynchronous FIFO Design	1
2.3	GALS Style of Communication	2
2.4	Wormhole Router Architecture Design	1
2.5	VC Router Architecture Design	2
2.6	Adaptive Router Architecture Design	1
3	**ROUTING ALGORITHM**	
3.1	Packet Routing	1
3.2	QOS, Congestion Control and Flow Control	1
3.3	Router Design	1
3.4	Network Link Design	1
3.5	Efficient and Deadlock	1
3.6	Free Tree-Based Multicast Routing Methods	1
3.7	Path-Based Multicast Routing For 2D and 3D Mesh Networks	1
3.8	Fault-Tolerant Routing Algorithms	1
3.9	Reliable and Adaptive Routing Algorithms	1
4		
4.1	Design-Security in Networks-On-Chips	2
4.2	Formal Verification of Communications in Networks-On Chips	3
4.3	Test and Fault Tolerance For Networks-On-Chip Infrastructures	2
4.4	Monitoring Services For Networks-On-Chips	2
5		
5.1	Three-Dimensional Networks-On-Chips Architectures	2
5.2	A Novel Dimensionally-Decomposed Router	2
5.3	Chip Communication in 3D Architectures	1
5.4	Resource Allocation For QOS On-Chip Communication	2
5.5	Networks-On-Chip Protocols Processor	1
5.6	Traffic Modeling For Networks- On-Chip	1
	Total	45

Course Designers

1. Mr.D.DHANASEKARAN – dhanasekarand@ksrct.ac.in

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60 PVL E26	WIRELESS SENSOR NETWORKS

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To understand the fundamentals of wireless sensor networks
- To familiarize with learning of the architecture of WSN
- To understand the concepts of MAC protocol in WSN
- To study the various routing protocols in WSN
- To understand the issues and challenges in security provisioning

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the fundamental concepts of wireless Sensor Networks and its applications	Understand
CO2	To gain knowledge about the sensor node and its architecture	Remember
CO3	Design and develop MAC Protocol	Apply
CO4	Illustrate the designing of various routing protocols	Apply
CO5	Analysis of various critical parameters in deploying a WSN	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3		3	
CO2	3	3	3		3	
CO3	3	3	3		3	
CO4	3	3	3		3	
CO5	3	3	3		3	

3- Strong;2-Medium;1-Some

Assessment Pattern

Cognitive Levels	Continuous Assessment Tests		End Semester Examination (Marks)
	1	2	
Remember	10	10	20
Understand	10	10	20
Apply	40	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-

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K.S.Rangasamy College of Technology–AutonomousR2022								
60 PVL E26- WIRELESS SENSOR NETWORKS								
M.E-VLSI DESIGN								
Semester	**Hours/Week**			**Total hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
II	3	0	0	45	3	40	60	100

Introduction to Wireless Sensor Networks: Introduction and overview of Wireless Sensor Networks (WSN), WSN Standards, IEEE 802.15.4, Zigbee, Category of Applications of WSN, Challenges for WSN, Enabling Technologies for WSN.	[9]
Single node Architecture: Hardware Components, Energy Consumption of Sensor nodes, Operating Systems and Execution Environments, Examples of Sensor Nodes, Network Architecture: WSN Scenarios, Optimization Goals and figures of Merits, Design principles for WSNs, Service Interfaces for WSNs, Gateway Concepts.	[9]
MAC Protocols: Fundamentals of MAC Protocols, MAC Protocols for WSNs, Contention-Based protocols: Power Aware Multi-Access with Signaling - Data-Gathering MAC, Contention-Free Protocols: Low-Energy Adaptive Clustering Hierarchy, B-MAC, S-MAC, Dissemination Protocol for Large Sensor Network.	[9]
Routing Protocols: Issues in designing a routing protocol, classification of routing protocols, table-driven, on-demand, hybrid, flooding, hierarchical, and power aware routing protocols.	[9]
QoS and Energy Management : Issues and Challenges in providing QoS, classifications, MAC, network layer solutions, QoS frameworks, need for energy management, classification, battery, transmission power, and system power management schemes.	[9]
TotalHours	**45**

TextBook(s):

1.	C. Siva Ram Murthy, and B. S. Manoj, "AdHoc Wireless networks ", Pearson Education - 2008.

Reference(s):

1.	Feng Zhao and LeonidesGuibas, "Wireless sensor networks ", Elsevier publication - 2004.
2.	Jochen Schiller, "Mobile Communications", Pearson Education, 2nd Edition, 2003.
3.	William Stallings, "Wireless Communications and Networks ", Pearson Education - 2004

Contents and Lecture Schedule

Module No.	Topic	No. of Hours
1	**Introduction to Wireless Sensor Networks**	
1.1	Introduction and overview of Wireless Sensor Networks (WSN)	1
1.2	WSN Standards	1
1.3	IEEE 802.15.4	1
1.4	Zigbee	1
1.5	Category of Applications of WSN	2
1.6	Challenges for WSN	1
1.7	Enabling Technologies for WSN	2
2	**Single node Architecture:**	
2.1	Hardware Components	1
2.2	Energy Consumption of Sensor nodes	1
2.3	Operating Systems and Execution Environments	1
2.4	Examples of Sensor Nodes	1

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2.5	Network Architecture: WSN Scenarios	1
2.6	Optimization Goals and figures of Merits	1
2.7	Design principles for WSNs	1
2.8	Service Interfaces for WSNs	1
2.9	Gateway Concepts	1
3	**MAC Protocols**	
3.1	Fundamentals of MAC Protocols	1
3.2	MAC Protocols for WSNs	1
3.3	Contention-Based protocols : Power Aware Multi-Access with Signaling	1
3.4	Data-Gathering MAC	1
3.5	Contention-Free Protocols	1
3.6	Low-Energy Adaptive Clustering Hierarchy	1
3.7	B-MAC	1
3.8	S-MAC	1
3.9	Dissemination Protocol for Large Sensor Network	1
4	**Routing Protocols:**	
4.1	Issues in designing a routing protocol	1
4.2	Classification of routing protocols	2
4.3	Table-driven, on-demand,	2
4.4	Hybrid, flooding	2
4.5	Hierarchical,	1
4.6	Power aware routing protocols	1
5	**QoS and Energy Management**	
5.1	Issues and Challenges in providing QoS	2
5.2	Classifications	1
5.3	MAC	1
5.4	Network layer solutions	1
5.5	QoS frameworks	1
5.6	Need for energy management	1
5.7	Classification, battery,	1
5.8	Transmission power, and system power management schemes.	1
	Total Hours	**45**

Course Designers

1. K.Rajasekar - rajasekark@ksrct.ac.in

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60 PAC 001	ENGLISH FOR RESEARCH PAPER WRITING

Category	L	T	P	Credit
AC	2	0	0	0

Objective

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand that how to improve your writing skills and level of readability
CO2	Learn about what to write in each section
CO3	Understand the skills needed when writing a Title
CO4	Understand the skills needed when writing the Conclusion
CO5	Ensure the good quality of paper at very first-time submission

Assessment Pattern

Bloom's Category	Continuous Assessment Tests(Marks)	
	1	2
Remember(Re)	10	10
Understand(Un)	20	20
Apply (Ap)	30	30
Analyze (An)	0	0
Evaluate(Ev)	0	0
Creative (Cr)	0	0
Total	60	60

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K.S.Rangasamy College of Technology – Autonomous R2022								
60 PAC 001 – English for Research Paper Writing								
Common to all Branches								
Semester	Hours/Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I /II	2	0	0	30	0	100	-	100

Introduction to Research Paper Writing Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	[6]
Presentation Skills Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction	[6]
Title Writing Skills Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check	[6]
Result Writing Skills Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	[6]
Verification Skills Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first time submission	[6]
Total Hours	**30**

Text Book(s):	
1.	Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2	Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
Reference(s):	
1.	Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
2.	Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.
3.	Phill Williams, Advanced Writing skills for students of English, Rumian Publishers, 2018
4.	Sudhir S. Pandhye, English Grammar and Writing Skills, Notion Press, 2017.

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60 PAC 002	DISASTER MANAGEMENT

Category	L	T	P	Credit
AC	2	0	0	0

Objective

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches Teach how to improve writing skills and level of readability

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Ability to summarize basics of disaster
CO2	Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3	Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4	Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5	Ability to develop the strengths and weaknesses of disaster management approaches

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)	
	1	2
Remember(Re)	10	10
Understand(Un)	20	20
Apply (Ap)	30	30
Analyze (An)	0	0
Evaluate(Ev)	0	0
Creative (Cr)	0	0
Total	60	60

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K.S. Rangasamy College of Technology – Autonomous R2022								
60 PAC 002 – Disaster Management								
Common to all Branches								
Semester	Hours/Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I/II	2	0	0	30	0	100	-	100

Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.	[6]
Repercussions of Disasters and Hazards Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	[6]
Disaster Prone Areas In India Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics	[6]
Disaster Preparedness and Management Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and other Agencies, Media Reports: Governmental and Community Preparedness.	[6]
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.	[6]
Total Hours	**30**

Text Book(s):

1.	Goel S. L., Disaster Administration and Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2	Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company,2007.

Reference(s):

1.	Sahni, Pardeep et.al.," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, 2001.
2.	Subramanian R,"Disaster Management", Vikas publishing Housing Pvt. Ltd., 2018.
3.	Chu-hua Kuei, Christian N Madu, Handbook of Disaster Management Risk Reduction & Management: Climate change and Natural Disaster, world scientific, 2017.
4.	Janki Andharia, Disaster studies: Exploring Intersectional ties in Disaster Discourse, Springer, 2020.

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60 PAC 003	CONTITUTION OF INDIA

Category	L	T	P	Credit
AC	2	0	0	0

Objective

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional. Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
CO2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India
CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
CO4	Discuss the passage of the Hindu Code Bill of 1956.
CO5	Discuss the role and functioning of election commission of India.

Assessment Pattern

Bloom's Category	Continuous Assessment Tests(Marks)	
	1	2
Remember(Re)	10	10
Understand(Un)	20	20
Apply (Ap)	30	30
Analyze (An)	0	0
Evaluate(Ev)	0	0
Creative (Cr)	0	0
Total	60	60

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K.S.Rangasamy College of Technology – Autonomous R2022								
60 PAC 003 – Constitution of India								
Common to all Branches								
Semester	Hours/Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I / II	2	0	0	30	0	100	-	100

History of Making of The Indian Constitution History, Drafting Committee, (Composition & Working)	[3]
Philosophy of The Indian Constitution Preamble, Salient Features	[3]
Contours of Constitutional Rights and Duties Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.	[6]
Organs of Governance Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.	[6]
Local Administration District's Administration head: Role and Importance Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Panchayat raj: Introduction, PRI: Zila Panchayat. Elected officials and their roles, CEO Zila Panchayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.	[6]
Election Commission Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.	[6]
Total Hours	**30**

Text Book(s):

1.	The Constitution of India,1950 (Bare Act),Government Publication.
2	Busi S N, Ambedkar B R, "Framing of Indian Constitution",1st Edition, 2015.

Reference(s):

1.	Jain, M P, "Indian Constitution Law", 7th Edition, Lexis Nexis,2014
2.	Basu, D D, "Introduction to the Constitution of India", Lexis Nexis, 2015.
3.	Bhansali S R., "Textbook on The Constitution of India", Universal Publishers, 2015
4.	Jain, M P., "Outlines of Indian Legal and Constitutional History", Lexis Nexis, 2014

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60 PVL 301	VLSI Signal Processing

Category	L	T	P	Credit
PC	3	0	0	3

Objective

- To learn the different types of Digital filters.
- To know the concepts of iteration bound.
- To learn the various transformations include retiming folding and unfolding.
- To acquire knowledge in pipelining and parallel processing.
- To learn the concepts of fast convolution and algorithmic strength reduction.

Prerequisite

Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design FIR and IIR digital filters	Remember, Understand, Apply
CO2	Apply various algorithms to compute iteration bound of DSP system	Apply
CO3	Describe the concepts of pipelining and parallel processing of FIR digital filters.	Remember, Understand, Apply
CO4	Design a high-level architectural transformation which includes retiming folding and unfolding	Apply, Analyze
CO5	Describe the techniques of fast convolution algorithm and architecture strength reduction in filters.	Apply

Mapping with Programme Outcomes

PO1	PO2	PO3	PO4	PO5	PO6
3	3	3	3	3	3
3	3	3	2	2	3
3	3	3	3	3	3
3	3	3	2	2	3
3	3	3	2	3	3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	15	15	30
Understand(Un)	15	15	30
Apply (Ap)	20	20	20
Analyze (An)	10	10	20
Evaluate(Ev)	0	0	0
Creative (Cr)	0	0	0

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Total	60	60	100

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K.S. Rangasamy College of Technology – Autonomous R 2022								
60 PVL 301- VLSI Signal Processing								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Realization Of Digital Filters FIR filter design - IIR filter design - Direct form I, II, Cascade, parallel, Ladder - Lattice filters.	[9]
Iteration Bound Introduction, Data flow graph representations, loop bound and iteration bound, Algorithms for computing Iteration bound, iteration Bound of multirate Data - Flow Graphs.	[9]
Pipelining And Parallel Processing Introduction - Pipelining of FIR Digital filters - Parallel processing - Pipelining and parallel processing for Low power.	[9]
Transformations RETIMING- Introduction - Definitions and Properties - Solving system of Inequalities - Retiming Techniques. UNFOLDING: Introduction - An algorithm for unfolding - Properties of unfolding - Critical path, unfolding and retiming - Application of unfolding. FOLDING: Introduction - folding Transformation - Register Minimization Techniques - Register Minimization in folded Architectures.	[9]
Fast Convolution Cook - Toom algorithm –modified Cook - Toom algorithm Winograd algorithm- modified Winograd algorithm, Algorithmic strength reduction in filters and transforms-parallel FIR filters, Parallel architectures for Rank-order filter.	[9]
Total hours	**45**

Text book(s):

1.	KeshabKParhi, 'VLSI Digital Signal Processing Systems Design and Implementation', Wiley - Inter science, 2008.
2.	John G Proakis and Dimitris G Manolakis, 'Digital signal processing – Principles, Algorithms and Applications', Pearson, 2011.

Reference(s):

1.	S.Y. Kuang, H.J. White house, T. Kailath, 'VLSI and Modern Signal Processing', Prentice Hall of India Private Ltd., 2013.
2.	Uwe Meyer Baese, 'Digital Signal Processing with Field Programmable Gate Arrays', Springer, 2014.
3.	Lonnie C Ludeman, 'Fundamentals of Digital Signal Processing', Wiley India (P) Ltd., 2009.
4.	Peter Pirsch 'Architectures for Digital Signal Processing', Wiley India (P) Ltd., 2009.

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Realization of Digital Filters**	
1.1	FIR Filter Design	1
1.2	IIR Filter Design	1
1.3	Direct form I Realization	1
1.4	Direct form II Realization	1
1.5	Cascade Realization	1

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1.6	Parallel Realization	1
1.7	Ladder form realization	1
1.8	Lattice filters	2
2		
2.1	Introduction	1
2.2	Data flow graph representations	2
2.3	loop bound and Iteration bound	2
2.4	Algorithms for computing Iteration bound	2
2.5	Iteration Bound of Multirate Data - Flow Graphs	2
3	**Pipelining and Parallel Processing**	
3.1	Introduction	1
3.2	Pipelining of FIR Digital filters	2
3.3	Parallel processing	2
3.4	Pipelining for Low power	2
3.5	Parallel processing for Low power	2
4	**Transformations**	
4.1	RETIMING- Introduction - Definitions and Properties	1
4.2	Solving system of Inequalities, Retiming Techniques	1
4.3	UNFOLDING: Introduction, An algorithm for unfolding	1
4.4	Properties of unfolding, Critical path, unfolding and retiming	1
4.5	Application of unfolding	1
4.6	FOLDING: Introduction	1
4.7	Folding Transformation	1
4.8	Register Minimization Techniques	1
4.9	Register Minimization in folded Architectures	1
5	**Fast Convolution**	
5.1	Introduction	1
5.2	Cook - Toom algorithm	1
5.3	Modified Cook - Toom algorithm	1
5.4	Winograd algorithm	1
5.5	Modified Winograd algorithm	1
5.6	Algorithmic strength reduction in filters and transforms	2
5.7	Parallel FIR filters	1
5.8	Parallel architectures for Rank-order filter.	1
	Total	45

Course Designers

1. Mr.S.Saravanan – saravanan.s@ksrct.ac.in

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60 PVL E31	DSP STRUCTURES FOR VLSI

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To understand the fundamentals of DSP
- To learn various DSP structures and their implementation.
- To know designing constraints of various filters
- Design and optimize VLSI architectures for basic DSP algorithms
- To enable students to design VLSI system with high speed and low power.

Prerequisite

Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquired knowledge about fundamentals of DSP processors.	Understand, Apply
CO2	Improve the overall performance of DSP system through various transformation and optimization techniques.	Understand, Apply
CO3	To understand the need of different types of instructions for DSP.	Understand, Apply
CO4	Optimize design in terms of computation complexity and speed.	Apply
CO5	Understand clock based issues and design asynchronous and wave pipelined systems.	Remember, Understand

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3		3
CO2	3	3	3	3		3
CO3	3	3	3	3		3
CO4	3	3	3	3		3
CO5	3	3	3	3		3

Assessment Pattern

Cognitive Levels	Continuous Assessment Tests		End Semester Examination(Marks)
	1	2	
Remember	10	10	10
Understand	10	20	30
Apply	40	30	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-

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Total	60	60	100

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60 PVL E31 – DSP STRUCTURES FOR VLSI								
M.E-VLSI DESIGN								
Semester	Hours / Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

INTRODUCTION TO DIGITAL SIGNAL PROCESSING Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG.	[9]
ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters parallel processing, pipelining and parallel processing for low power.	[9]
RETIMING, UNFOLDING AND FOLDING Retiming: definitions, properties and problems- solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications of Unfolding, Folding transformation register minimization techniques, register minimization in folded architecture- folding of multirate system.	[9]
FAST CONVOLUTION Cook-toom algorithm- modified cook-Toom algorithm. Design of fast convolution algorithm by inspection - Winograd algorithm- modified Winograd algorithm.	[9]
ARITHMETIC STRENGTH REDUCTION IN FILTERS Parallel FIR filters-fast FIR algorithms-two parallel and three parallel. Parallel architectures for rank order filters -odd-even, merge-sort architecture-rank order filter architecture-parallel rank order filters-running order, merge order sorter, low power rank order filter.	[9]
Total Hours	**45**

Reference(s):

1. K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.

Course Contents and Lecture Schedule

Module No.	Topic	No. of Hours
1	**INTRODUCTION TO DIGITAL SIGNAL PROCESSING**	
1.1	Linear system theory , convolution and correlation	1
1.2	DFT & FFT	2
1.3	Basic concepts in FIR filters and IIR filters	2
1.4	Filter realizations	2
1.5	Representations of DSP algorithms- block diagram, SFG, DFG.	2
2	**ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER**	
2.1	Data-flow graph representations	1

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2.2	Loop bound and Iteration bound algorithms for computing iteration bound	2
2.3	LPM algorithm	2
2.4	Ppipelining of FIR digital filters parallel processing,	2
2.5	Pipelining and parallel processing for low power	2
3	**RETIMING, UNFOLDING AND FOLDING**	
3.1	Retiming: definitions, properties and problem solving systems of inequalities	2
3.2	Properties of Unfolding, critical path, Unfolding and Retiming	2
3.3	Applications of Unfolding	1
3.4	Folding transformation register minimization techniques	2
3.5	Register minimization in folded architecture	1
3.6	Folding of multirate system	1
4	**FAST CONVOLUTION**	
4.1	Cook-toom algorithm	2
4.2	modified cook-Toom algorithm	2
4.3	Design of fast convolution algorithm	2
4.4	Byinspection - Winograd algorithm	2
4.5	Modified Winograd algorithm	1
5	**ARITHMETIC STRENGTH REDUCTION IN FILTERS**	
5.1	Parallel FIR filters	1
5.2	Fast FIR algorithms-two parallel and three parallel	2
5.3	Parallel architectures for rank order filters -odd-even	2
5.4	Merge-sort architecture-rank order filter architecture	1
5.5	Parallel rank order filters	1
5.6	Running order merge order sorter	1
5.7	Low power rank order filter	1
	Total Hours	**45**

Course Designers

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60 PVL E32	APPLIED MEDICAL IMAGE PROCESSING

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To introduce the fundamentals of image processing techniques
- To apply the enhancement techniques and analyse the image
- To learn about medical image representation
- To analyse the quality of medical image and do classification
- To study about image registrations and visualizations

Prerequisite

NIL

CourseOutcomes

On the successful completion of the course, students will be able to

CO1	Explain the fundamentals of image processing	Remember, Understand
CO2	Analyze Morphology, enhancement techniques and implement these in image	Apply
CO3	Understand the representation of medical images	Understand Apply
CO4	Analyze medical images of numerous modalities such as PET, MRI, CT, or microscopy	Apply, Analyse
CO5	Study image registrations and visualization	Understand, Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		2	
CO2	3		3	2	3	
CO3	3		3	2	3	
CO4	3		3	2	3	
CO5	3		3	2	3	

Assessment Pattern

Bloom'sCategory	ContinuousAssessmentTests (Marks)		End Sem Examination(Marks)
	1	2	
Remember	10	10	30
Understand	20	20	30
Apply	30	25	30
Analyse	0	5	10
Evaluate	0	0	0
Create	0	0	0
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E32- APPLIED MEDICAL IMAGE PROCESSING								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

IMAGE FUNDAMENTALS Image perception, MTF of the visual system, Image fidelity criteria, Image model, Image sampling and quantization – two dimensional sampling theory, Image quantization, Optimum mean square quantizer, Image transforms – DFT, DCT, KLT,SVD.	[9]
IMAGE ENHANCEMENT AND RESTORATION Histogram equalization and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic mean filters, Homomorphic filtering, Color image enhancement. Image Restoration - degradation model, Unconstrained and constrained restoration, Inverse filtering- Wiener filtering.	[9]
MEDICAL IMAGE REPRESENTATION Pixels and voxels – algebraic image operations - gray scale and color representation- depth-color and look up tables - image file formats- DICOM- other formats- Analyze 7.5, NifTI and Interfile, Image quality and the signal to noise ratio.	[9]
MEDICAL IMAGE ANALYSIS AND CLASSIFICATION Image segmentation- pixel based, edge based, region based segmentation. Image representation and analysis, Feature extraction and representation, Statistical, Shape, Texture, feature and image classification – Statistical, Rule based, Neural Network approaches.	[9]
IMAGE REGISTRATIONS AND VISUALIZATION Rigid body visualization, Principal axis registration, Interactive principal axis registration, Feature based registration, Elastic deformation based registration, Image visualization – 2D display methods, 3D display methods, virtual reality based interactive visualization.	[9]
Total hours	**45**

Text book(s):

1. Atam P.Dhawan, 'Medical Image AnalysisII', Wiley Interscience Publication, NJ, USA, 2nd edition 2011.
2. Anil. K. Jain, 'Fundamentals of Digital Image Processing', Pearson education, Indian Reprint 2003.

Reference(s):

1. John L.Semmlow,'Biosignal and Biomedical Image Processing Matlab Based applications', Marcel Dekker Inc.,New York,2004
2. Kavyan Najarian and Robert Splerstor, 'Biomedical signals and Image processing', CRC – Taylor and Francis, New York, 2006
3. R.C.Gonzalez and R.E.Woods, 'Digital Image Processing', Second Edition, Pearson Education, 2002.

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Course Contents and Lecture Schedule

S.No	Topic	No.of Hours	Mode of content Delivery
1	**IMAGE FUNDAMENTALS**		
1.1	Image perception	1	BB
1.2	MTF of the visual system	1	BB
1.3	Image fidelity criteria	1	BB
1.4	Image model	1	PPT
1.5	Image sampling and quantization	1	PPT
1.6	Two dimensional sampling theory	1	FC
1.7	Image quantization, Optimum mean square quantizer	1	PPT
1.8	Image transforms – DFT, DCT	1	PPT/SL
1.9	KLT,SVD	1	BB
2	**IMAGE ENHANCEMENT AND RESTORATION**		
2.1	Histogram equalization and specification techniques	1	FC
2.2	Noise distributions,	1	PPT
2.3	Spatial averaging, Directional Smoothing,	1	PPT
2.4	Median, Geometric mean, Harmonic mean,	1	FC
2.5	Contra harmonic mean filters, Homomorphic filtering	1	SL
2.6	Color image enhancement	1	PPT
2.7	Image Restoration - degradation model,	1	PPT
2.8	Unconstrained and constrained restoration	1	PPT
2.9	Inverse filtering- Wiener filtering	1	PPT
3	**MEDICAL IMAGE REPRESENTATION**		
3.1	Pixels and voxels – algebraic image	2	PPT
3.2	Operations - gray scale and color representation	1	PPT
3.3	Depth-color and look up tables	1	PPT
3.4	Image file formats	1	PPT
3.5	DICOM- other formats	1	SL
3.6	Analyze 7.5 NifTI and Interfile	2	Case study
3.7	Image quality and the signal to noise ratio	1	
4	**MEDICAL IMAGE ANALYSIS AND CLASSIFICATION**		
4.1	Image segmentation	1	PPT
4.2	Pixel based, edge based, region based segmentation	2	PPT
4.3	Image representation and analysis	1	PPT
4.4	Feature extraction and representation	2	FC
4.5	Statistical, Shape, Texture, feature	1	PPT
4.6	Image classification	1	SL

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4.7	Neural Network approaches	1	Seminar
5	**IMAGE REGISTRATIONS AND VISUALIZATION**		
5.1	Rigid body visualization	2	PPT
5.2	Principal axis registration	1	PPT
5.3	Interactive principal axis registration	1	PPT
5.4	Feature based registration	1	PPT
5.5	Elastic deformation based registration	1	PPT
5.6	Image visualization – 2D display methods, 3D display methods	1	FC
5.7	virtual reality based interactive visualization	2	SL Solving

Course Designers

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

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60 PVL E33	DATA SCIENCE AND ENGINEERING

Category	L	T	P	Credit
PE	3	0	0	3

Objective

- To understand the concepts and technologies in data science
- To explore the concepts in statistical inference and exploratory data analysis
- To understand the basic machine learning algorithms
- To explore the effective visualization of given data using visualization tools
- To implement the data science applications

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the basics of Data Sciences	Understand
CO2	To know the mathematical foundations needed for data Science and perform Exploratory Data Analysis.	Remember, Understand
CO3	Implement models such as k-nearest Neighbors, Naive Bayes, linear and logistic Regression, decision trees, neural networks and clustering.	Apply
CO4	Create effective visualization of given data	Apply
CO5	Build data science applications	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3		3	
CO2	3	3	3		3	
CO3	3	3	3		3	
CO4	3	3	3		3	
CO5	3	3	3		3	

Assessment Pattern

Cognitive Levels	Continuous Assessment Tests		End Semester Examination (Marks)
	1	2	
Remember	10	10	20
Understand	10	10	20
Apply	40	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K. S. Rangasamy College of Technology – Autonomous R2022								
60 PVL E33-DATA SCIENCE AND ENGINEERING								
M.E-VLSI DESIGN								
Semester	Hours / Week			Total hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Introduction to core concepts and technologies: Introduction, Terminology, Data-Properties of Data, Types of data, Why Data Science? Computer Science, Data Science, and Real Science, data science process, Data Acquisition and Data Science Life Cycle, Ethics in Data Science, data science toolkit, Example applications. Data wrangling: Sources of data, Data collection and API, Working with data: Reading Files, Cleaning Data.	[8]
Statistical Inference, Exploratory Data Analysis: Statistical thinking in Data Science, Statistical Inference, Statistical Analysis, Modeling, Exploratory data analysis and data visualization, Missing value analysis, The correction matrix, Outlier detection analysis.	[9]
Basic Machine Learning Algorithms: Brief introduction, Linear / Polynomial Regression, Logistic Regression, Classification, Regularization, Support vector machines, Extreme learning machines, Naive Bayes, Cross Validation, Label Encoding, Random Forests, Decision Trees, Clustering, Dimensionality reduction, Manifold learning, 2D/3D Convolution, Introduction to Neural Networks, Evaluation Metrics.	[10]
Data visualization: Introduction, Types of data visualization, Data Visualization – Basic principles, ideas and tools for basic data visualization tools (plots, graphs and summary)-Data Extraction and Filtering Visualization Principles. Data visualization Tool: Random Sample Generation using Tableau, Remote Database connectivity, Creating charts, Mapping data in Tableau, create your own visualization of a complex dataset in Tableau.	[10]
Applications of Data Science: Case Studies of Data Science Application, Recommended Systems on Real World Data Sets, Weather forecasting, Stock market prediction, Object recognition, Matching Skills to Job.	[8]
Total Hours	**45**

Text Book(s):

1. Cathy O'Neil, Rachel Schutt, Doing Data Science, Straight Talk from The Frontline. O'Reilly, 2013
2. Joel Grus, "Data Science from Scratch: First Principles with Python", O'Reilly Media

Reference(s):

1. Jure Leskovek, Anand Rajaraman, Jeffrey Ullman, Mining of Massive Datasets. v2.1, Cambridge University Press, 2014.
2. Aurelien Geron, "Hands-On Machine Learning with Scikit-Learn and Tensor Flow: Concepts, Tools, and Techniques to Build Intelligent Systems", 1st Edition, O'Reilly Media
3. Jiawei Han and Jian Pei, "Data Mining Concepts and Techniques", Third Edition, Morgan Kaufmann Publishers
4. Jain V.K., "Data Sciences", Khanna Publishing House, Delhi.
5. https://onlinecourses.nptel.ac.in/noc21_cs23/

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Course Contents and Lecture Schedule

Module No.	Topic	No. of Hours
1	**Introduction to core concepts and technologies**	
1.1	Introduction, Terminology, Data-Properties of Data, Types of data	1
1.2	Why Data Science? Computer Science, Data Science, and Real Science, data science process	1
1.3	Data Acquisition and Data Science Life Cycle	1
1.4	Ethics in Data Science, data science toolkit, Example applications.	2
1.5	Data wrangling: Sources of data	1
1.6	Data collection and API	1
1.7	Working with data: Reading Files, Cleaning Data.	1
2	**Statistical Inference, Exploratory Data Analysis:**	
2.1	Statistical thinking in Data Science	1
2.2	Statistical Inference, Statistical Analysis, Modeling	2
2.3	Exploratory Data Analysis & Data visualization	2
2.4	Missing value analysis	2
2.5	The correction matrix, Outlier detection analysis	2
3	**Basic Machine Learning Algorithms**	
3.1	Brief introduction, Linear / Polynomial Regression, Logistic Regression	1
3.2	Classification, Regularization	1
3.3	Support vector machines, Extreme Learning Machnies,Naive Bayes	2
3.4	Cross Validation, Label Encoding	1
3.5	Random Forests, Decision Trees	1
3.6	Clustering, Dimensionality reduction	1
3.7	Manifold learning, 2D/3D Convolution	1
3.8	Introduction to Neural Networks	1
3.9	Evaluation Metrics.	1
4	**Data visualization**	
4.1	Introduction, Types of data visualization, Data Visualization	1
4.2	Basic principles, ideas and tools for basic data visualization tools (plots, graphs and summary statistics)-	2
4.3	Data Extraction and Filtering, Data Visualization Principles.	2
4.4	Data visualization Tool: Random Sample Generation using Tableau, Remote Database connectivity	2
4.5	Creating charts	1
4.6	Mapping data in Tableau	1
4.7	create your own visualization of a complex dataset	1
5	**Applications of Data Science:**	
5.1	Case Studies of Data Science Application	2
5.2	Recommended Systems on Real World Data Sets	1
5.3	Weather forecasting	1
5.4	Stock market prediction	2
5.5	Object recognition	1
5.6	Matching Skills to Job	1
	Total Hours	**45**

Course Designers

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1. K.Gogila Devi - gogiladevi@ksrct.ac.in

60 PVL E34	ASIC Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objective

- To know on the types of ASIC design and ASIC library design
- To introduces the principles of design logic cells, I/O Cells and Interconnect architecture
- To analyse various programmable ASIC architecture with logic cells, I/O Cells and Interconnect architecture
- To analyse high performance algorithms for floor planning and placement and routing of cells in ASIC design
- To deal with the entire FPGA and ASIC design flow from the circuit and layout design point of view

Prerequisite

Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply logical effort technique for predicting delay, delay minimization and FPGA architectures	Apply
CO2	Design logic cells and I/O cells	Apply
CO3	Analyze the various resources of recent FPGAs	Analyze
CO4	Use algorithms for floor planning and placement of cells, routing for optimization of power and speed and understand the concept of layout static time analyses	Apply
CO5	Analyze high performance algorithms available for ASICs	Analyze

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1						3
CO2				2		3
CO3	3	2	3	2	3	3
CO4	3	2	3	3	2	3
CO5	2			3		3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		Model Exam (Marks)	End Sem Examination (Marks)
	1	2		
Remember (Re)	10	10	10	10
Understand (Un)	35	35	60	60
Apply (Ap)	10	10	20	20
Analyse (An)	5	5	10	10
Evalute (Ev)	-	-	-	-
Create (Cr)	-	-	-	-

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Total	60	60	100	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E34-ASIC Design								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

INTRODUCTION TO ASIC'S, CMOS LOGIC AND ASIC LIBRARY DESIGN Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.	[9]
PROGRAMMABLE ASIC'S, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS Anti Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.	[9]
PROGRAMMABLE ASIC ARCHITECTURE Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.	[9]
LOGIC SYNTHESIS, STATIC TIMING ANALYSIS, PLACEMENT AND ROUTING Logic Synthesis, Pre-Layout STA, Floor Planning Goals and Objectives, Floor Planning Tools, I/O Placement and Power Planning, Standard Cell Placement, Clock Tree Synthesis, Timing Optimization, Routing: Global Routing and Detailed Routing, , post-layout STA.	[9]
SYSTEM-ON-CHIP DESIGN SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.	[9]
Total hours	**45**

Text book(s):	
1.	M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2.	Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science,2006.
Reference(s):	
1.	Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, "FPGA-Based Implementation of Signal Processing Systems", Wiley, 2008.
2.	J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009.
3.	David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, "Low Power Methodology Manual: For System-on-Chip Design (Integrated Circuits and Systems) " Springer, 2008.
4.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN**	
1.1	Types of Asics	2
1.2	Design Flow - CMOS Transistors	2
1.3	Combinational Logic Cell	1
1.4	Sequential Logic Cell	1

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1.5	Data Path Logic Cell	1
1.6	Transistors as Resistors - Transistor Parasitic Capacitance	1
1.7	Logical Effort	1
2	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	
2.1	Anti Fuse - Static Ram - EPROM and EEPROM Technology	2
2.2	ACTEL ACT	1
2.3	Xilinx LCA	1
2.4	ALTERA FLEX	1
2.5	ALTERA MAX	1
2.6	DC & AC Inputs and Outputs	1
2.7	Clock & Power Inputs	1
2.8	Xilinx I/O Blocks	1
3	**PROGRAMMABLE ASIC ARCHITECTURE**	
3.1	Architecture and Configuration of ARTIX	2
3.2	Cyclone and KINTEX Ultra Scale	2
3.3	STRATIX FPGA	2
3.4	Micro-Blaze / NIOS Based Embedded Systems	2
3.5	Signal Probing Techniques	1
4	**LOGIC SYNTHESIS, STATIC TIMING ANALYSIS, PLACEMENT AND ROUTING**	
4.1	Logic Synthesis, Pre-Layout STA	1
4.2	Floor Planning Goals and Objectives, Floor Planning Tools	1
4.3	I/O Placement and Power Planning, Standard Cell Placement	2
4.4	Clock Tree Synthesis, Timing Optimization	2
4.5	Routing: Global Routing and Detailed Routing	1
4.6	Post-layout STA	2
5	**SYSTEM-ON-CHIP DESIGN**	
5.1	SoC Design Flow	1
5.2	Platform-Based and IP Based SoC Designs	2
5.3	Basic Concepts of Bus-Based Communication Architectures	1
5.4	High Performance Filters using Delta-Sigma Modulators	2
5.5	Case Studies: Digital Camera, SDRAM, High Speed Data standards.	3
	Total	45

Course Designers

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60 PVL E35	MIXED SIGNAL VLSI DESIGN	Category	L	T	P	Credit
		PE	3	0	0	3

Objective

- To know the types of filters for VLSI circuits.
- To explain the different techniques of ADC for mixed signal circuits.
- To introduce the different techniques of DAC for mixed signal circuits.
- To learn about sigma delta converters for mixed signal circuits.
- To learn the design methodologies and EDA tools for mixed signal VLSI circuits

Prerequisite

Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the concept of different filter for VLSI circuit design	Remember, Understand Apply
CO2	Explain the function of continuous time filter in MOS technology for mixed signal circuits	Remember, Understand Apply
CO3	Apply DAC and ADC techniques for data conversions using CMOS technologies	Apply
CO4	Illustrates the concept of sigma delta converter method for VLSI circuits	Remember, Understand Apply
CO5	Design a complete mixed signal system using EDA tools	Analyze

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	3		3
CO2	3	3	3	3		3
CO3	3	3	3	3	3	3
CO4	3		2	3	2	3
CO5	3	3	3	3	3	3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		Model Marks (100)	End Sem Examination (Marks)
	1	2		
Remember (Re)	12	10	20	20
Understand (Un)	38	40	60	60
Apply (Ap)	10	10	20	20
Analyse (An)	-	-	-	-

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Evalute (Ev)	-	-	-	-
Create (Cr)	-	-	-	-
Total	60	60	100	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E35- MIXED SIGNAL VLSI DESIGN								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Introduction to Active Filters & Switched Capacitor Filters Switched Capacitor (SC) circuits: Parasitic Insensitive Switched Capacitor amplifiers-Switched capacitor filters and resistors – comparators - CMOS, BiCMOS sample-and-holds - Linearity, noise in switched capacitor circuits – Integrator- Biquadratic SC Filter- SC N-path filters.	[9]
Continuous Time Filters Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors –BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance -Elementary transconductor building block- First and second order filters.	[9]
Digital to Analog & Analog to Digital Converters Types of DAC's: Current switched, Resistive, Current cell design in current steering DAC, Hybrid converters, segmented converters DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, folding ADC's, Multiple-Bit Pipeline ADCs and SAR ADC, time-interleaved A/D converters	[9]
Sigma Delta Converters Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's- discrete delta sigma modulator-based ADC using MATLAB	[8]
Analog and Mixed Signal Extensions to HDL Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples-analog extensions to Verilog: Mixed Signal HDL design Flow- data types –Expressions – Signals- Analog behavior – Hierarchical Structures –Mixed signal Interaction	[10]
Total hours	**45**

Text book(s):

1.	David A Johns and Ken Martin, 'Analog Integrated Circuit Design', John Wiley and Sons, 2016.
2.	Rudy van de Plassche, 'Integrated Analog-to-Digital and Digital-to-Analog Converters', Kluwer, 2014.

Reference(s):

1.	Behzad Razavi, 'Design of Analog CMOS Integrated Circuits', 2012
2.	Michael D.Ciletti, 'Advanced Digital Design with the Verilog HDL', 2nd Edition, Pearson Education, 2011
3.	Antoniou, 'Digital Filters Analysis and Design', Tata McGraw Hill, 2010
4.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

Course Contents and Lecture Schedule

S.No.	Topic	No. of Hours
1	**Introduction to Active Filters & Switched Capacitor Filters**	
1.1	Switched Capacitor (SC) circuits: Parasitic Insensitive Switched Capacitor amplifiers	2
1.2	Switched capacitor filters and resistors – comparators	2
1.3	CMOS, BiCMOS sample-and-holds	2

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1.4	Linearity, noise in switched capacitor circuits	1
1.5	Integrator- Biquadratic SC Filter	1
1.6	SC N-path filters.	1
2	**Continuous Time Filters**	
2.1	Introduction to Gm - C filters	1
2.2	Bipolar transconductors	1
2.3	CMOS Transconductors using Triode transistors, active transistors	2
2.4	BiCMOS transconductors	1
2.5	MOSFET C Filters - Tuning Circuitry	1
2.6	Dynamic range performance- Elementary transconductor building block	2
2.7	First and second order filters	1
3	**Digital to Analog & Analog to Digital Converters**	
3.1	Types of DAC's: Current switched, Resistive, Current cell design in current steering DAC	2
3.2	Hybrid converters, segmented converters DAC's	2
3.3	Techniques for improving linearity - Analog to Digital Converters	1
3.4	Quantization errors - non-idealities - types of ADC's: Flash, folding ADC's	2
3.5	Multiple-Bit Pipeline ADCs and SAR ADC, time-interleaved A/D converters	2
4	**Sigma Delta Converters**	
4.1	Over sampled converters - over sampling without noise & with noise	2
4.2	Implementation imperfections - first order modulator	2
4.3	Decimation filters - second order modulator	1
4.4	Sigma delta DAC & ADC's	2
4.5	Discrete delta sigma modulator-based ADC using MATLAB	1
5	**Analog and Mixed Signal Extensions to HDL**	
5.1	Introduction - Language design objectives - Theory of differential algebraic equations	1
5.2	The 1076 .1 Language - Tolerance groups	1
5.3	Tolerance groups - Conservative systems - Time and the simulation cycle	2
5.4	A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples	2
5.5	Analog extensions to Verilog: Mixed Signal HDL design Flow- data types –Expressions	2
5.6	Signals- Analog behavior –Hierarchical Structures –Mixed signal Interaction	2
	Total	45

Course Designers

1. Ms.R.Ramya – rramya@ksrct.ac.in

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60 PVL E41	System Verilog	Category	L	T	P	Credit
		PE	3	0	2	4

Objective

- To understand the basic concept of System Verilog for Verification
- To understand advanced verification features used in System Verilog
- To know the threads and inter-process communication and functional coverage
- To apply System Verilog Concepts to do synthesis, analysis and architecture design
- To understand the purpose of hardware-software Verification

Prerequisite

Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Use System Verilog to create correct, efficient, and re-usable models for digital designs	Remember, Understand Apply
CO2	Use System Verilog to create test-benches for digital design	Apply
CO3	Understand the terminology and concept of OOPS in System Verilog for verification	Remember, Understand
CO4	Understand the inter-process communication between modules in System Verilog	Remember, Understand
CO5	Design a complete system model using System Verilog	Analyze

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3			3		3
CO2	3			3		3
CO3	3			3	3	3
CO4	3			3	2	3
CO5	3	2	3	3	3	3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		Model Exam (Marks)	End Sem Examination (Marks)
	1	2		
Remember (Re)	10	10	20	20
Understand (Un)	40	40	60	60
Apply (Ap)	10	10	20	20
Analyse (An)	-	-	-	-
Evalute (Ev)	-	-	-	-
Create (Cr)	-	-	-	-

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Total	60	60	100	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E41- System Verilog								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	60	4	40	60	100

VERIFICATION METHODOLOGY Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Test-bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test-bench Components, Layered Test-bench.	[12]
SYSTEM VERILOG BASICS AND CONCEPTS Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types With Typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions.	[12]
OOPS Introduction-Where to Define a Class- OOPS Terminology -Creating New Objects -Object De-allocation- Using Objects -Static Variables Vs. Global Variables -Class Routines -Defining Routines Outside of The Class - Scoping Rules -Using One Class Inside Another - Understanding Dynamic Objects -Copying Objects -Public Vs. Private -Straying Off Course - Building a Testbench.	[12]
THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE Working With Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Testbench With Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analysing Coverage Data, Measuring Coverage Statistics.	[12]
COMPLETE DESIGN MODEL USING SYSTEM VERILOG- CASE STUDY System Verilog ATM Example, Data Abstraction, Interface Encapsulation, Design Top Level Squat, Receivers and Transmitters, Test Bench for ATM.	[12]
PRACTICAL EXERCISES: 1. Design a Testbench for 2x1 Mux Using Gates 2. Implementation of a Mailbox By Allocating Memory 3. Implementation and Testing of Semaphore for a Simple DUT 4. Implementation of Scoreboard for a Simple DUT	
Total hours	**60**

Text book(s):	
1.	System Verilog for Verification: a Guide to Learning The Testbench Language Features, Chris Spear,Springer 2006
2.	Writing Testbenches: Functional Verification of HDL Models, Second Edition, Janick Bergeron, Kluwer Academic Publishers, 2003.
Reference(s):	
1.	System Verilog for Design: a Guide to Using System Verilog for Hardware Design and Modeling, 2 nd Edition, Stuart Sutherland, Simon Davidman and Peter Flake, Springer
2.	Open Verification Methodology Cookbook, Mark Glasser, Springer, 2009
3.	Assertion-Based Design, 2nd Edition, Harry D. Foster, Adam C. Krolnik, David J. Lacey, Kluwer Academic Publishers, 2004.
4.	Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**UNIT I VERIFICATION METHODOLOGY**	
1.1	Verification Guidelines: Introduction	2
1.2	Verification Process, Verification Plan	2
1.3	Verification Methodology Manual	2
1.4	Basic Test-bench Functionality	2
1.5	Directed Testing, Methodology Basics	2
1.6	Constrained-Random Stimulus, Functional Coverage	1
1.7	Test-bench Components, Layered Test-bench	1
2	**UNIT II SYSTEM VERILOG BASICS AND CONCEPTS**	
2.1	Data Types: Built-in Data Types, Fixed-Size Arrays	2
2.2	Dynamic Arrays, Queues	2
2.3	Creating New Types With Typedef	2
2.4	Creating User-Defined Structures	1
2.5	Enumerated Types, Constants, Strings	1
2.6	Procedural Statements and Routines: Procedural Statements	2
2.7	Tasks, Functions, and Void Functions	2
3	**UNIT III OOPS**	
3.1	Introduction-Where to Define a Class	2
3.2	OOPS Terminology	2
3.3	Creating New Objects -Object De-allocation- Using Objects	2
3.4	Static Variables Vs. Global Variables -Class Routines	1
3.5	Defining Routines Outside of The Class	1
3.6	Scoping Rules -Using One Class Inside Another	1
3.7	Understanding Dynamic Objects -Copying Objects	1
3.8	Public Vs. Private -Straying Off Course	1
3.9	Building a Testbench	1
4	**UNIT IV THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE**	
4.1	Working With Threads	1
4.2	Inter-Process Communication	1
4.3	Events, Semaphores, Mailboxes	1
4.4	Building a Testbench With Threads and IPC	1
4.5	Coverage Types, Functional Coverage Strategies	2

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4.6	Simple Functional Coverage Example, Coverage Options	2
4.7	Parameterized Cover Groups	2
4.8	Analysing Coverage Data, Measuring Coverage Statistics	2
5	**UNIT V COMPLETE DESIGN MODEL USING SYSTEM VERILOG- CASE STUDY**	
5.1	System Verilog ATM Example	2
5.2	Data Abstraction	2
5.3	Interface Encapsulation	2
5.4	Design Top Level Squat	2
5.5	Receivers and Transmitters	2
5.6	Test Bench for ATM	2
	Total	60

Course Designer

1. Mrs.C.Saranya – saranyac@ksrct.ac.in

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60 PVL E42	HDL for IC Design	Category	L	T	P	Credit
		PE	3	0	2	4

Objective

- To understand the basics of Verilog HDL
- To design digital systems using the different modeling
- To understand the HDL synthesis
- To learn verification process
- To test the design using testbench

Prerequisite

Digital System Design, Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply digital design concepts and write Verilog programs	Remember, Understand, Apply
CO2	Write Verilog programs using dataflow and behavioral modeling	Apply, Create
CO3	Synthesis the digital design for implementation in FPGA	Understand, Apply
CO4	Understand the principles of verification process and System Verilog	Apply, Analyze
CO5	Interface testbench and design under test	Apply, Analyze

Mapping with Programme Outcomes

PO1	PO2	PO3	PO4	PO5	PO6
3	3	3	3	3	3
3	3	3	3	3	3
3	3	3	3	3	3
3	3	3	3	3	3
3	3	3	3	3	3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Knowledge (Kn)	20	20	30
Apply (Ap)	20	20	30
Analyse (An)	10	10	20
Evaluate(Ev)	0	0	0
Create (Cr)	10	10	20

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Total	60	60	100

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60 PVL E42- HDL for IC Design								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	60	4	40	60	100

Introduction to Verilog Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Verilog Operators and Modules-Verilog Ports, Data types and Assignments-Gate level modeling-Switch level modeling-Modeling of CMOS gates and Boolean functions.	[12]
Dataflow and behavioral modeling Basics of dataflow modeling-Review of flip-flops-Verilog modeling of flip-flops-Basics of behavioral modeling-Verilog modeling of counters, sequence detector, FSMs and shift registers.	[12]
Verilog HDL Synthesis Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis - FIR filter implementation-IIR filter implementation.	[12]
Introduction to System Verilog Verification Process- Basic Testbench Functionality - Directed Testing - Constrained-Random Stimulus, Functional Coverage, Testbench Components- Layered Testbench- Building a Layered Testbench- Simulation Environment Phases - Data types and procedural statements: Built-In Data Types- Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays- Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion- Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine.	[12]
Connecting the Test bench and Design Separating the Test bench and Design-The Interface Construct-Stimulus Timing-Interface Driving and Sampling-Connecting It All Together-Top-Level Scope-Program - Module Interactions-System Verilog Assertions-The Four-Port ATM Router.	[12]
PRACTICAL EXERCISES: 1. Simulate the Combinational circuits using different modeling 2. Design and implement FSM 3. Design and implement FIR and IIR filter 4. Verify the digital systems using system verilog	
Total hours	**60**

Text book(s):

1	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education New Delhi, 2019
2	Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2nd Edition, Springer, 2012.

Reference(s):

1	https://ocw.mit.edu - Massachusetts Institute of Technology Open Courseware.
2	Michael D Ciletti - Advanced Digital Design with the Verilog HDL, 2nd Edition, PHI, 2009
3	Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Introduction to Verilog**	
1.1	Overview of digital design using Verilog HDL	2
1.2	Hierarchical Modeling concepts	2
1.3	Verilog Operators and Modules	2
1.4	Verilog Ports, Data types and Assignments	1
1.5	Gate level modelling	1
1.6	Switch level modelling	1
1.7	Modelling of CMOS gates	1
1.8	Boolean functions	2
2	**Dataflow and behavioral modelling**	
2.1	Basics of dataflow modelling	2
2.2	Review of flip-flops	2
2.3	Verilog modeling of flip-flops	2
2.4	Basics of behavioral modelling	1
2.5	Verilog modeling of counters	1
2.6	Sequence Detector	1
2.7	Finite State Machine (FSM)	2
2.8	Shift Registers	1
3	**Verilog HDL Synthesis**	
3.1	Synthesis Design Flow	2
3.2	Verification of the gate level net list	4
3.3	Modeling for logic synthesis	4
3.4	Example of sequential circuit synthesis	2
3.5	FIR filter implementation-IIR filter implementation	2
4	**Introduction to System Verilog**	
4.1	Verification Process- Basic Testbench Functionality	1
4.2	Directed Testing - Constrained-Random Stimulus	2
4.3	Functional Coverage, Testbench Components	1
4.4	Layered Testbench- Building a Layered Testbench	2
4.5	Simulation Environment Phases	2
4.6	Data types and procedural statements: Built-In Data Types	1
4.7	Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays	1
4.8	Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion	1
4.9	Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine	1
5	**Connecting the Test bench and Design**	
5.1	Separating the Test bench and Design	2
5.2	The Interface Construct	2
5.3	Stimulus Timing	2
5.4	Interface Driving	1
5.5	Sampling-Connecting It All Together	1

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5.6	Top-Level Scope-Program	1
5.7	Module Interactions	1
5.8	System Verilog Assertions	1
5.9	The Four-Port ATM Router	1
	Total	60

Course Designers

1. Mr.S.Saravanan – saravanan.s@ksrct.ac.in

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60 PVL E43	Deep Learning	Category	L	T	P	Credit
		PE	3	0	2	4

Objective

The aim of the course is

- To present the mathematical, statistical and computational challenges of building neural Networks,
- To study the concepts of back propagation & optimization algorithms,
- To introduce dimensionality reduction techniques,
- To study different deep neural networks and
- To study the optimization of deep networks

Prerequisite

Machine Learning Techniques

CourseOutcomes

On the successful completion of the course, students will be able to

CO1	Learn the basics of deep learning	Remember, Understand
CO2	Implement ANN using back propagation algorithm	Apply
CO3	Analyze high dimensional data using reduction techniques	Apply, Analyse
CO4	Explain the architecture of different CNNs	Understand
CO5	Study optimization and generalization in deep learning	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		2	
CO2	3		3	2	3	
CO3	3		3	2	3	
CO4	3		3	2	3	
CO5	3		3	2	3	

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	30
Understand	20	20	30
Apply	30	25	30
Analyse	0	5	10
Evaluate	0	0	0
Create	0	0	0
Total	60	60	100

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60 PVL E43- Deep Learning								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	60	4	40	60	100

Introduction Introduction to machine learning - Perceptrons, logistic regression - Introduction to Neural Nets: What a shallow network computes - Training a network: loss functions, back propagation and gradient descent – representation power of Feed forward Neural Networks **Practical: Implementation of Logistic Regression using sklearn**	[12]
Backpropagation and optimization algorithms Back propagation and regularization, Gradient Descent (GD), Momentum based GD, Nestero Accelerated GD, Stochastic GD, Adagrad, RMSProp, Adam, Eigen values and Eigen vectors. **Practical: Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets.**	[12]
Dimentionality Reduction Principal Component Analysis and its interpretations, Singular value decomposition - Auto encoders and relation to PCA, Regularization in auto encoders, Denoising auto encoders, Sparse auto encoders, and Contractive auto encoders, Regularization, Data set augmentation, dropout. **Practical: Study the effect of batch normalization and dropout in neural network classifier**	[12]
Convolution Neural Networks : Architectures – AlexNet, VGGNet, SegNet, ResNet - Training a: weights initialization, batch normalization, Deep dream, Deep Art, Fooling Convolution neural network **Practical: Image segmentation using ResNet / SegNet**	[12]
Optimization and Generalization Optimization in deep learning – Non-convex optimization for deep networks - Stochastic Optimization- Generalization in neural networks - Spatial Transformer Networks- Recurrent networks, LSTM - Recurrent Neural Network Language Models. **Practical: Write a program to construct a Bayesian network considering medical data.**	[12]
Total hours	**60**

Text book(s):

1	Deng & Yu, Deep Learning: Methods and Applications, Now Publishers, 2013
2	Ian Goodfellow, Yoshua Bengio, Aaron Courville, Deep Learning, MIT Press, 2016

Reference(s):

1.	Michael Nielsen, Neural Networks and Deep Learning, Determination Press, 2015
2.	Cosma Rohilla Shalizi, Advanced Data Analysis from an Elementary Point of View, 2015
3.	Francois Chollet, “Deep learning with Python” – Manning Publications

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Course Contents and Lecture Schedule

S.No	Topic	No.of Hours
1	**Introduction**	
1.1	Introduction to machine learning	1
1.2	Perceptrons	1
1.3	Logistic regression	2
1.4	Introduction to Neural Nets: What a shallow network computes?	2
1.5	Training a network: loss functions,	2
1.6	Back propagation and gradient descent	2
1.7	Representation power of Feed forward Neural Networks	2
2	**Backpropagation and optimization algorithms**	
2.1	Back propagation and regularization	2
2.2	Gradient Descent (GD),	2
2.3	Momentum based GD	2
2.4	Nestero Accelerated GD	1
2.5	Stochastic GD	1
2.6	Adagrad	1
2.7	RMSProp	1
2.8	Adam	1
2.9	Eigen values and Eigen vectors.	1
3	**Dimentionality Reduction**	
3.1	Principal Component Analysis and its interpretations	1
3.2	Singular value decomposition	1
3.3	Auto encoders and relation to PCA	1
3.4	Regularization in auto encoders	2
3.5	Denoising auto encoders	2
3.6	Sparse auto encoders,	2
3.7	Contractive auto encoders	2
3.8	Regularization, Data set augmentation	1
3.9	Dropout	1
4	**Convolution Neural Networks :**	
4.1	Architectures – AlexNet	2
4.2	VGGNet	2
4.3	SegNet	2
4.4	ResNet	2
4.5	Training a: weights initialization, batch normalization	1
4.6	Deep dream	1
4.7	Deep Art	1
4.8	Fooling Convolution neural network	1

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5	**Optimization and Generalization**	
5.1	Optimization in deep learning	2
5.2	Non-convex optimization for deep networks	2
5.3	Stochastic Optimization	2
5.4	Generalization in neural networks	2
5.5	Spatial Transformer Networks	1
5.6	Recurrent networks	1
5.7	LSTM	1
5.8	Recurrent Neural Network Language Models	1

CourseDesigners

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

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60 PVL E44	ADAPTIVE SIGNAL PROCESSING

Category	L	T	P	Credit
PE	3	0	2	4

Objective

- To understand the concepts of stationary and non-stationary random signals and characterization of discrete-time random processes.
- To explain Non parametric and parametric methods for power spectrum estimation.
- To design optimum filters such as Wiener and Kalman filters.
- To design adaptive filtering techniques using LMS and RLS algorithm and understand the applications of adaptive filters.
- To learn the concepts of Continuous Wavelet Transform and its applications.

Prerequisite

Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the mathematical description and signal modelling of discrete time random processes.	Remember, Understand, Apply
CO2	Apply various techniques for estimating the power spectrum of a stationary random Process.	Remember, Understand, Apply
CO3	Design different optimum filters	Analyse
CO4	Design, implementation and analysis of FIR adaptive filters and application of adaptive filters.	Understand, Analyse
CO5	Discuss the concepts of CWT and its applications.	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3		3	3	
CO2	3	3			3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3			3	
3- Strong;2-Medium;1-Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember(Re)	20	10	10
Understand(Un)	20	20	40
Apply (Ap)	20	20	40
Analyse (An)	0	10	10
Evalute(Ev)	0	0	0

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Create (Cr)	0	0	0

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60 PVL E44- Adaptive Signal Processing								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	60	4	40	60	100

Discrete time random signals Discrete random processes-Definitions-Ensemble Averages-Stationary processes- Auto covariance and Autocorrelation matrices-Properties- Ergodicity- White noise- Weiner Khitchine relation- Power spectral density –Filtering random processes- Spectral Factorization Theorem- Special types of random processes – ARMA, AR, MA Processes-Pade approximation – Prony's method. **Practical** : Power spectral density using square magnitude and autocorrelation method.	[12]
Spectrum Estimation Non-Parametric methods: Periodogram - Performance of the Periodogram, Modified periodogram, Barlett'smethod, Welch's method and Blackman-Tukey Approach- Performance comparisons -Parametric methods - AR, MA, ARMA spectrum estimation using YuleWalker method- The Levinson-Durbin recursion- Development of the Recursion-The Levinson recursion algorithm for solving Toeplitz system of equations. **Practical :** Estimate the PSD of a noisy signal using periodogram and modified periodogram.	[12]
Optimum Filters Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter-Filtering, Linear Prediction- IIR Wiener filter-Causal and Non causal IIR Wiener filter-Discrete Kalman filter. Practical : Application of optimum filters	[12]
Adaptive Filters FIR Adaptive filters - Newton's steepest descent method - Widrow-Hoff LMS Adaptive algorithm - Normalized LMS algorithm- Applications - Noise cancellation - Channel equalization – Echo cancellation- Adaptive Recursive Filters - RLS adaptive algorithm **Practical Lab**:Adaptive Filter for noise cancellation in Sinusoidal signal and System Identification using Adaptive filter	[12]
Continuous Wavelet transform Wavelet basis– STFT- Continuous time Wavelet Transform (CWT)– Principles of Multi-Resolution Analysis (MRA) - Construction of Wavelets-Construction of Orthonormal Wavelets-Applications of wavelet transform - noise reduction, image compression. **Practical :** Time-Frequency Analysis with the Continuous Wavelet Transform and Signal Reconstruction from Continuous Wavelet Transform Coefficients.	[12]
Total hours	**60**

Text book(s):

1. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling', John Wiley and Sons Inc., New York, 2008.
2. Jaideva C Goswami and Andrew K Chan, 'Fundamentals of Wavelets–Theory, Algorithms and Applications', John Wiley &Sons, Inc., Singapore, 2011.

Reference(s):

1. Alan V Oppenheim, Ronald W Schafer, 'Discrete Time Signal Processing', Pearson Education India, 3rd Edition, 2014.
2. John G. Proakis, Dimitris G. Manolakis, 'Digital Signal Processing: Principles, Algorithms and Applications', Pearson Education, 4th Edition,2014.
3. Simon Haykin, 'Adaptive Filter Theory', Pearson, 5th Edition, 2013.
4. Steven M.Kay,' Modern Spectrum Estimation: Theory And Application', Prentice Hall PTR, 1999.

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Course Contents and Lecture Schedule

S.No	Topic	No.of Hours
1	**Discrete time random signals**	
1.1	Discrete random processes Definitions, Ensemble Averages, Stationary processes	2
1.2	Auto covariance and Autocorrelation matrices-Properties Ergodicity	2
1.3	White noise Weiner Khitchine relation Power spectral density	2
1.4	Filtering random processes: Spectral Factorization Theorem	2
1.5	Special types of random processes: ARMA, AR, MA Processes	2
1.6	Pade approximation	1
1.7	Prony's method.	1
2	**Spectrum Estimation**	
2.1	Non-Parametric methods: Periodogram Performance of the Periodogram	2
2.2	Modified periodogram Barlett'smethod	2
2.3	Welch's method and Blackman-Tukey Approach Performance comparisons	2
2.4	Parametric methods : AR, MA, ARMA spectrum estimation using Yule Walker method-	2
2.5	The Levinson-Durbin recursion- Development of the Recursion.	2
2.6	The Levinson recursion algorithm for solving Toeplitz system of equations.	2
3	**Optimum Filters**	
3.1	(LMMSE) Filtering: Wiener Hopf Equation	2
3.2	FIR Wiener filter	2
3.3	Filtering & Linear Prediction	2
3.4	IIR Wiener filter-Causal IIR Wiener filter	2
3.5	Non causal IIR Wiener filter	2
3.6	Discrete Kalman filter.	2
4	**Adaptive Filters**	
4.1	FIR Adaptive filters - Newton's steepest descent method	2
4.2	Widrow-Hoff LMS Adaptive algorithm	2
4.3	Normalized LMS algorithm	2
4.4	Noise cancellation, Channel equalization, Echo cancellation-	4
4.5	Adaptive Recursive Filters : RLS adaptive algorithm	2
5	**Continuous Wavelet transform**	
5.1	Wavelet basis STFT	2
5.2	Continuous time Wavelet Transform (CWT)	2
5.3	Principles of Multi-Resolution Analysis (MRA)	2

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5.4	Construction of Wavelets	1
5.5	Construction of Orthonormal Wavelets	1
5.6	Applications of wavelet transform : noise reduction, image compression.	2
	Total	60

Course Designers

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60 PVL E45	MEMS system design

Category	L	T	P	Credit
PE	3	0	2	4

Objective

- To introduce and provide a broad view of MEMS and micro systems.
- To familiarize with the fundamentals of MEMS products, materials for microsystems
- To learn the microsystem fabrication process
- To learn the various MEMS-specific design issues and constraints will be discussed in detail
- To know the applications of micro sensors and micro actuators

Prerequisite

Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the basic principles of MEMS sensors and actuators.	Remember Understand
CO2	Outline the various materials used for MEMS products.	Understand Analyze
CO3	Familiarize with the fabrication process of MEMS devices.	Remember, Analyze
CO4	Analyze the design process in mems systems.	Analyze
CO5	Know the diverse applications of MEMS sensors	Remember, Understand

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3			
CO2	3	3	3			
CO3	3		3		3	
CO4	3	3	3	3		
CO5	3	3	3		3	

Assessment Pattern

Bloom's Category	Continuous Assessment Tests(Marks)		End Sem Examination(Marks)
	1	2	
Remember(Re)	10	10	30
Understand(Un)	10	10	10
Apply (Ap)	20	20	30
Analyse (An)	10	10	15
Evalute(Ev)	0	0	0
Create (Cr)	10	10	15
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R 2022								
60 PVL E45 – MEMS system design								
M.E-VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	60	4	40	60	100

INTRODUCTION Overview – MEMS and micro system products – Microsystems and Microelectronics – Working Principle of Microsystems – Micro actuation techniques. Practical: **D**esign and Analysis of Capacitive Accelerometer.	[12]
MATERIALS FOR MICROSYSTEMS Substrate and wafer – single crystal silicon wafer formation – ideal substrates – Mechanical properties – silicon compounds – Sio2, SiC, Si3N4 and polycrystalline silicon – Silicon piezo resistors – Gallium arsenide - quartz – Piezoelectric crystals - polymers. Practical: Estimation of Resistance change in SOI Piezo-resistive Pressure Sensor	[12]
MICRO SYSTEM FABRICATION PROCESS Photolithography – photo resist- Ion implantation – Diffusion – oxidation – CVD – physical vapor deposition- Deposition by epitaxy – etching process. Practical: Study of IntelliSuite Software for the design and fabrication process of MEMS devices	[12]
MICRO SYSTEM DESIGN Design considerations- Process design- mask layout design – Design constraints – Selection of Materials – Manufacturing Process - Signal transduction – packaging – Application of Micro system in automotive industry – Biomedical – Aerospace – telecommunication. Practical: Design and Analysis of Piezoresistive Accelerometer using Coventor Ware software.	[12]
MICRO SENSORS Introduction – Microsensors – Biomedical sensors – Pressure sensors – Thermal Sensors – Chemical sensors – Optical sensors – Microactuation – MEMS with actuators. Practical : simulation of Microsensors	[12]
Total hours	**60**

Text book(s):

1. Tai-Ran Hus, 'MEMS & Microsystems Design, Manufacture and Nanoscale engineering', John Wiley & Sons, 2013
2. Julian W.Gardner, Vijay K.Varadan, Osama O.Awadel Karim, 'Microsensors MEMS and Smart Devices', John Wiley & sons, 2011

Reference(s):

1. Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2012
2. Stephen D Senturia, 'Microsystem Design', Springer Publication, 2000
3. James J.Allen, Micro Electro Mechanical System Design, CRC Press Publisher, 2005
4. Thomas M.Adams and Richard A.Layton, 'Introduction MEMS, Fabrication and Application,' Springer,2010

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Course Content and Lecture Schedule

S.No	Topic	No. of Hours
1	**INTRODUCTION**	
1.1	Overview	2
1.2	MEMS	2
1.3	Microsystems	2
1.4	Micro system products	1
1.5	Microelectronics	1
1.6	Compare Microelectronics and Microsystems	1
1.7	Working Principle of Microsystems	1
1.8	Micro actuation techniques	1
1.9	Applications of MEMS	1
2	**MATERIALS FOR MICROSYSTEMS**	
2.1	Substrate and wafer	1
2.2	single crystal silicon wafer formation	1
2.3	ideal substrates	1
2.4	Mechanical properties	1
2.5	silicon compounds	1
2.6	Sio2, SiC, Si3N4 and polycrystalline silicon	1
2.7	Silicon piezo resistors	2
2.8	Gallium arsenide, quartz	2
2.9	Piezoelectric crystals, polymers	2
3	**MICRO SYSTEM FABRICATION PROCESS**	
3.1	Photolithography	1
3.2	photo resist	1
3.3	Ion implantation	1
3.4	Diffusion	2
3.5	oxidation	1
3.6	CVD	2
3.7	physical vapor deposition	2
3.8	Deposition by epitaxy	1
3.9	etching process	1
4	**MICRO SYSTEM DESIGN**	
4.1	Design considerations	1
4.2	Process design	2
4.3	mask layout design	2
4.4	Design constraints, Selection of Materials	1
4.5	Manufacturing Process	1
4.6	Signal transduction, packaging	1
4.7	Application of Micro system in automotive industry	2

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4.8	Biomedical	2
4.9	Aerospace, telecommunication.	
5	**MICRO SENSORS**	
5.1	Introduction	2
5.2	Microsensors	2
5.3	Biomedical sensors	1
5.4	Pressure sensors	1
5.5	Thermal Sensors	2
5.6	Chemical sensors	1
5.7	Optical sensors	1
5.8	Microactuation	1
5.9	MEMS with actuators	1
	Total	60

Course Designers

1. Baranidharan T - baranidharan@ksrct.ac.in

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60 PVL 3P1	Project Work I

Category	L	T	P	Credit
CG	0	0	12	6

Objective

- To impart practical knowledge to the students and also to make them to carry out the technical procedures in their project work.
- To provide an exposure to the students to refer, read and review the research articles, journals and conference proceedings relevant to their project work and placing this as their beginning stage for their final presentation
- Independently carry out research / investigation and development work to solve practical problems in the field of VLSI
- Write and present a substantial technical report / document in the field of VLSI
- Demonstrate the Research findings the VLSI area

Prerequisite

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Survey the relevant literature such as books, national/international refereed journals and contact resource persons for the selected topic of research.	Apply
CO2	Use different experimental techniques/different software/ computational/analytical tools.	Apply
CO3	Design and develop an experimental set up/ equipment/test rig.	Apply
CO4	Conduct tests on existing setups/equipment's and draws logical conclusions from the results after analyzing them.	Apply
CO5	Work in a research environment or in an industrial environment	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
1- low, 2- medium, 3- high						

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60 PVL 3P1-Project Work I								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
III	0	0	12	180	6	100	-	100

Methodology	• Project should be selected based on an IEEE paper which would be base paper • The paper has to be implemented fully • Modification has to be proposed on the base paper • Report has to be prepared by the students as per the format • Every week a report on the progress of the project has to be submitted (Friday/Saturday) by the student with the supervisor's signature • Three reviews will be conducted by a committee of minimum three members one of which should be the guide • Each review has to be evaluated for 100 marks • Attendance is compulsory for all reviews. If a student fails to attend the review for some valid reason with proper intimation, one or more chance may be given, else review mark will be zero • Internal evaluation has to be done for 100 marks

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60 PVL 4P1	Project Work II

Category	L	T	P	Credit
CG	0	0	24	12

Objective

- To impart practical knowledge to the students and also to make them to carry out the technical procedures in their project work.
- To provide an exposure to the students to refer, read and review the research articles, journals and conference proceedings relevant to their project work
- Independently carry out research / investigation and development work to solve practical problems in the field of VLSI
- Write and present a substantial technical report / document in the field of VLSI
- Demonstrate the Research findings the VLSI area

Prerequisite

Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop attitude of lifelong learning and interpersonal skills to deal with people working in diversified fields.	Apply
CO2	Synthesize knowledge and skills previously gained and apply to an in-depth study and execution of new technical problems in the area of VLSI.	Apply
CO3	Define specification, adopt new VLSI methodologies and analyze to produce a suitable research design and justify the design.	Apply
CO4	Demonstrate the research findings through hardware and software tools.	Apply
CO5	Present the findings of their technical solution in a written report and Publish the work in reputed journals and International Conferences.	Apply

Mapping with Programme Outcomes

Cos	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
1- low, 2- medium, 3- high						

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50 PVL 4P1 - PROJECT WORK – PHASE II								
M.E-VLSI Design								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
IV	0	0	24	360	12	60	40	100
Methodology	• The modification proposed in Phase I has to be implemented • Three reviews will be conducted by a committee of minimum three members one of which will be the guide • Each review has to be evaluated for 100 marks • Attendance is compulsory for all reviews. If a student fails to attend the review for some valid reason with proper intimation, one or more chance may be given, else review markwill be zero • They should publish the paper preferably in the journals/conferences • Final review will be done by the committee that consists of minimum three members one of which should be the guide(including one external expert examiner) • The report should be submitted by the students at the end of May							

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